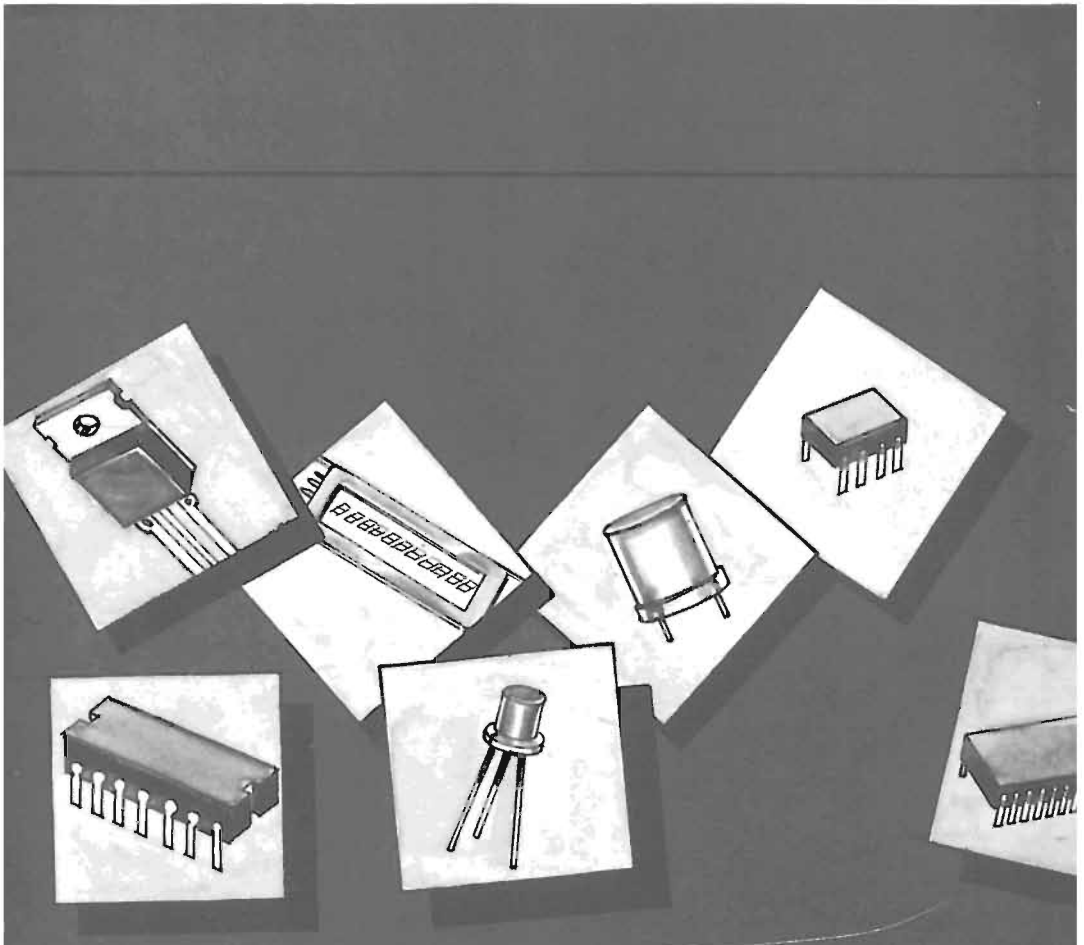
Electronic components and materials

PHILIPS

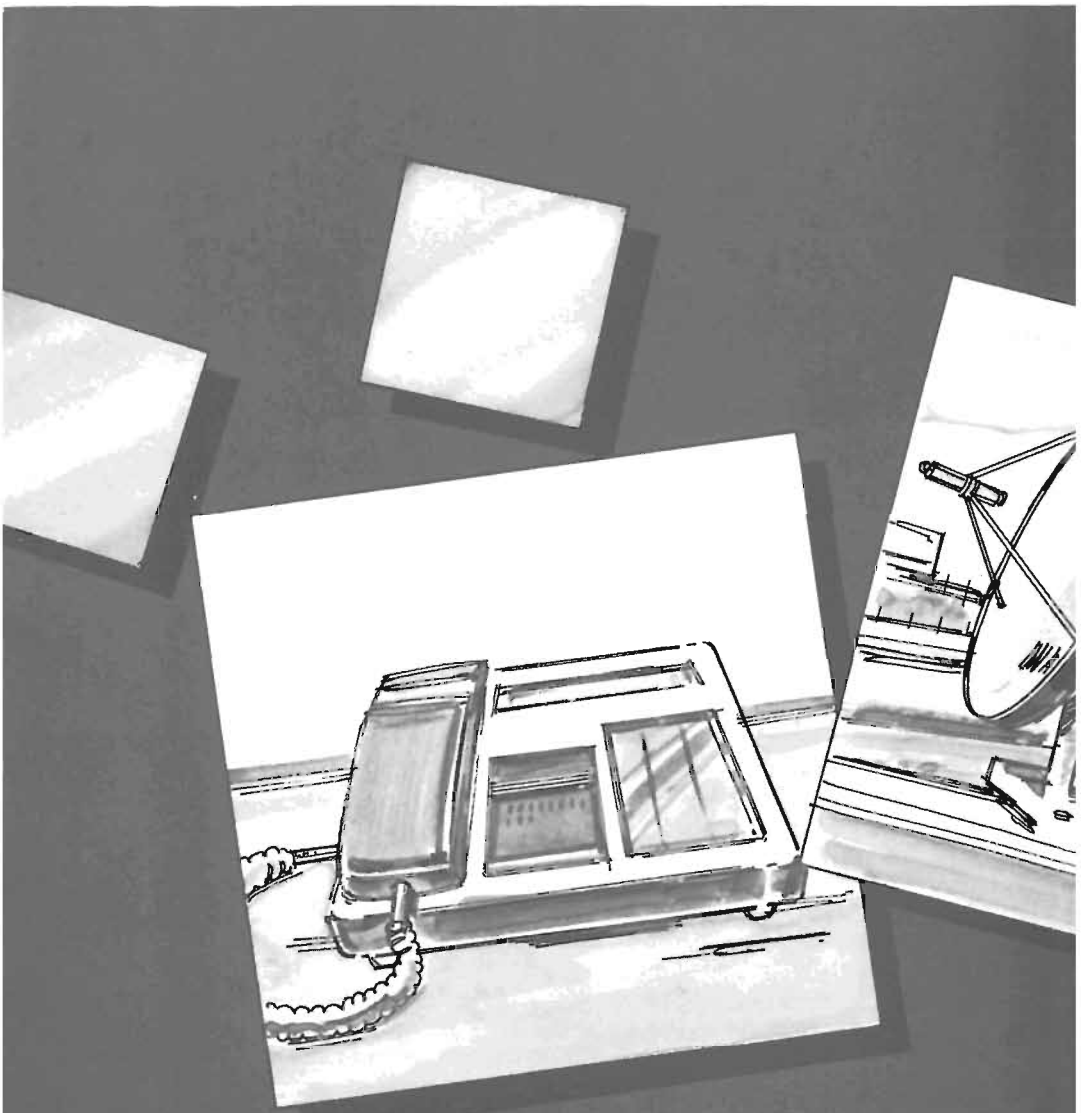
Components

for telephony



This catalogue is intended for electronic engineers involved in the design of telephony equipment. It includes only those components likely to be of direct interest.
When selecting a component supplier Philips is the natural choice. We are backed by worldwide research resources, plus development, application and quality laboratories. Our in depth knowledge, our command of proven technologies and our unequalled mass-production experience, plus our firm commitment to meeting the needs of the industrial and professional sectors, mean that when dealing with us, you deal with a partner, not just a supplier.

Recognizing the specific needs of the telephony industry, we are well aware of the need for an intensive dialogue between equipment and component manufacturers.
Detecting and keeping pace with system trends is a prerequisite to the development of new, advanced components. Components that will be required to provide a system life of 25 to 30 years.
If you are seeking such a dialogue, contact Philips, the company with the broadest technological base in the industry, and the one with a proven record in innovation, in high quality and in high volume production.

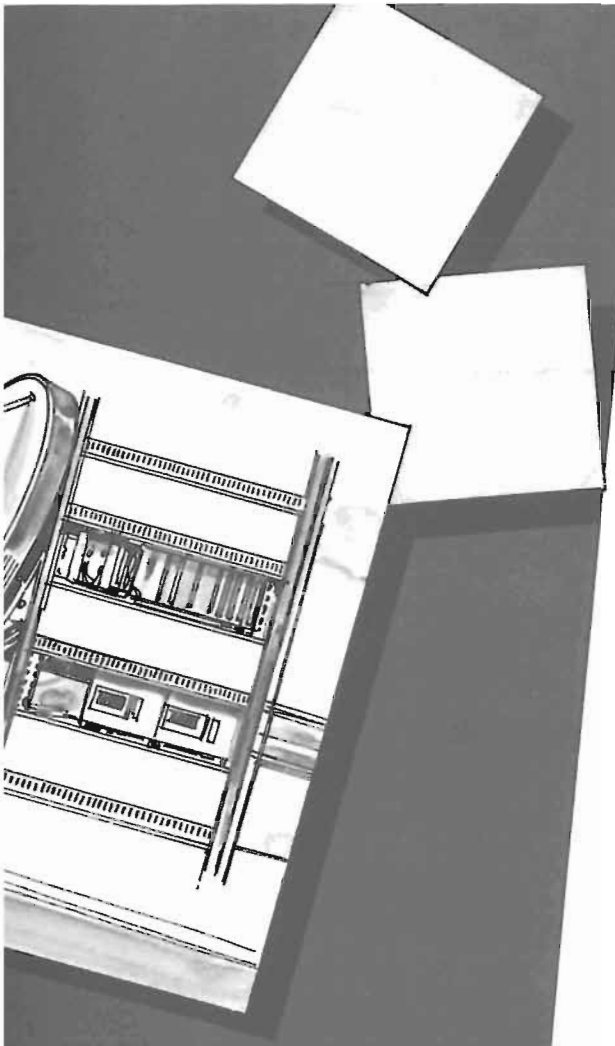


SUBSCRIBER

Revolutionary changes in subscriber-set design have greatly increased the scope and quality of the services offered. We offer many components for this and the next generation of subscriber equipment. Noteworthy are ICs for line current interrupt dialling or two-tone dialling, ringing, speech/transmission ICs, and a special microcomputer with peripherals such as two-tone diallers, RAM and LCD drivers.

For the future Integrated Services Digital Network, we have some special ICs in development – particularly for the digital subscriber set.

Besides ICs we offer dedicated components for over-voltage protection, quartz crystals, some special MOSFETs, loudspeakers and a complete LCD module.



EXCHANGE

It is in exchanges that the real impact of electronics is going to be felt in the coming years, and virtually all the standard electronic components you will need for design and manufacture will be available.

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BIPOLAR ICs FOR TELEPHONE SUBSCRIBER SETS

CMOS ICs FOR TELEPHONE SUBSCRIBER SETS

OTHER COMPONENTS FOR TELEPHONE SUBSCRIBER SETS

OTHER COMPONENTS FOR TELEPHONY

DEDICATED INTEGRATED CIRCUITS FOR TELEPHONE SETS

Introduction

Over the past ten years advances in microcircuit technology have resulted in the development of microprocessors, memories, and dedicated ICs that are now beginning to replace the traditional components of the subscriber set, to the benefit of both its performance and appearance.

For example, ICs for interrupted current-loop dialling (decadic or pulse) and for dual-tone multi-frequency (DTMF) dialling allow the dial to be replaced by a push-button keyboard. And by replacing the carbon microphone with an active type (electret or electro-dynamic) and using an electronic anti-sidetone circuit, the speech and transmission functions can be performed by an IC. Speech and dialling functions can also be integrated onto a single chip. In addition, the bell will eventually be replaced by an electronically driven transducer with a variety of ringing tones.

Microcircuits also allow incorporation of a host of new features such as automatic redialling, repertory dialling, automatic emergency-call dialling, dialled number display, tariff-unit metering, speech synthesis, hands-free and cordless telephone operation, and possibly a limited amount of data handling.

Research is also progressing into developing an Integrated Services Digital Network (ISDN), in which digitized voice, circuit-switched data and digital signalling combined with packet switched data can be processed. This trend will lead to the development of ICs for interface and protocol functions (firstly in office communication systems, and eventually in the public network).

The long life of existing equipment and the fact that their manufacture is often automated, means that several years must elapse whilst new components prove their operational and economic superiority to the telephone authorities. Many of the new components will therefore have to work alongside the old ones, and the order and speed of approach to all-electronic subscriber equipment will not necessarily be the same in all countries. We have therefore produced, or are developing the wide range of microcircuits listed on page 1 for telephones of the present and future. We also offer a range of components for protection against lightning and mains contact, MOS transistors for current loop interruption, quartz crystals, loudspeakers and a complete LCD module. In addition, we are developing a wide range of components for the subscriber line card, and for the ISDN.

ARCHITECTURE OF ELECTRONIC SUBSCRIBER SETS

The first step in converting subscriber sets to electronic operation will usually be replacement of the rotary dial by a pushbutton keyboard operating in conjunction with either a pulse generator for interrupted current-loop dialling or a tone generator for DTMF dialling. This effectively divides electronic telephone production into two main streams – one for sets with pulse dialling and one for sets with tone dialling. Subsequent steps are replacement of the carbon microphone by an active transducer such as an electret or electrodynamic microphone, and replacement of the transformer hybrid by an integrated speech/transmission circuit. The sequence continues with the inclusion of features such as repertory dialling, last-number redial, extended redial, dialled number display, and tariff-unit metering. There will also be some sets capable of either pulse or DTMF dialling.

The ringer is a completely separate function and can therefore be replaced by electronics at any stage.

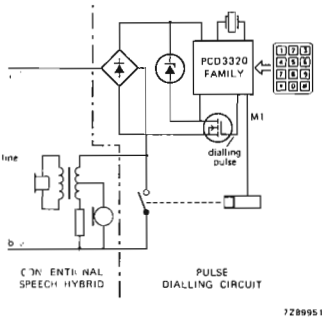
Telephones for pulse dialling

Fig. 1 opposite shows the architecture of three basic pushbutton subscriber sets for interrupted current-loop dialling using the PCD 3320 family of ICs.

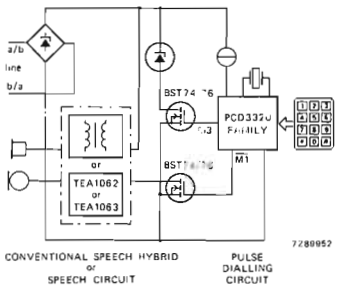
Fig. 1a shows an insert unit to perform the dial function in a conventional set with a transformer hybrid. The muting relay inhibits the speech function during dialling.

Fig. 1b shows a parallel circuit in which the line current flows through either the speech part or a dummy load, and is interrupted by the M3 output of the dialling IC. Note: the conventional speech circuit operating on two wires may be replaced by a speech circuit without electronic muting (TEA 1062/1063). This allows the possibility of operating the speech IC in the handset with only a two-wire cable.

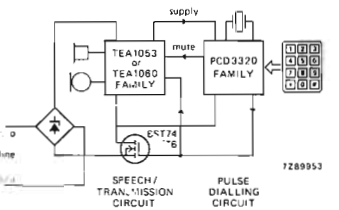
In Fig. 1c the dialling IC operates in conjunction with a transmission IC with common-line interface. The latter works with either an electret or an electrodynamic microphone and has a special input for muting. For this function we have a variety of speech/transmission ICs (TEA 1042, 1053, 1054, 1055, 1060 and 1061).



(a) Pulse dial insert unit replacing the rotary dial. in a conventional telephone set.



(b) Pulse dial basic set with either conventional or electronic speech.



(c) Pulse dial basic set with two ICs and common line interface.

Fig.1 Subscriber set architecture for current loop interrupt dialling (excluding ringer, cradle contact, polarity guard & protection.

Telephones for DTMF dialling

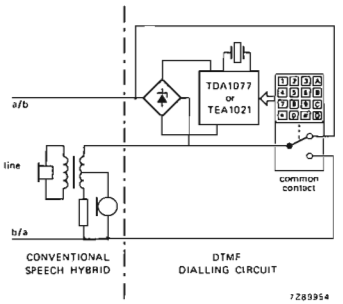
Fig. 2 shows the architecture of four basic push-button sets for DTMF dialling.

In Fig. 2a a DTMF insert replaces the rotary dial. This requires a DTMF generator with output stage and voltage stabilizer, e.g. the TEA 1077 or its improved successor the TEA 1021, both of which require a common contact to switch between speech and dialling.

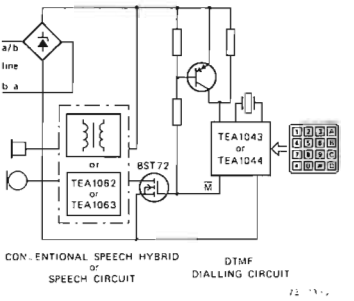
In Fig. 2b the electronic mute output of the TEA 1043/TEA 1044 enables electronic switching from dialling to speech, using a single-contact keyboard. As in Fig. 1b, electronic speech circuits like the TEA 1062 and 1063 may replace conventional ones.

In Fig. 2c a CMOS DTMF generator operates in conjunction with the speech/transmission circuit with electronic muting. This incorporates a voltage stabilizer and an audio output stage for both speech and DTMF signals. Note, the range of speech/transmission ICs referred to above in connection with Fig. 1c can also be used in this application.

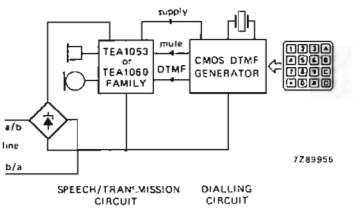
Fig. 2d shows the application of a combined DTMF/transmission circuit, the TEA 1046. Unlike the TEA 1042/53/54/55/60/61/62 and 63, the TEA 1046 has no line current controlled gain. It does, however, offer an economic solution for simple DTMF subscriber sets.



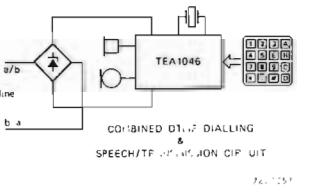
(a) DTMF insert unit replacing the rotary dial in a conventional telephone set.



(b) DTMF basic set with either conventional speech or electronic speech.



(c) DTMF basic set with two ICs and common line interface.



(d) Electronic speech and DTMF on a single chip.

Fig.2 Subscriber-set architecture for dual-tone multi-frequency (DTMF) dialling (excluding ringer, cradle contact, polarity guard & protection).

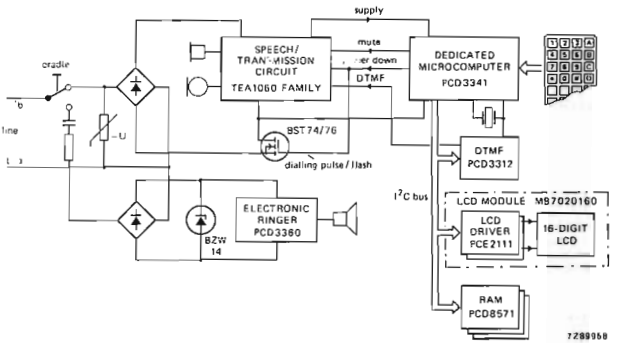
Telephones with extended features

Fig. 3a shows a subscriber set with additional features such as last-number redial, extended redial, repertory dialling, register recall and dialled number display.

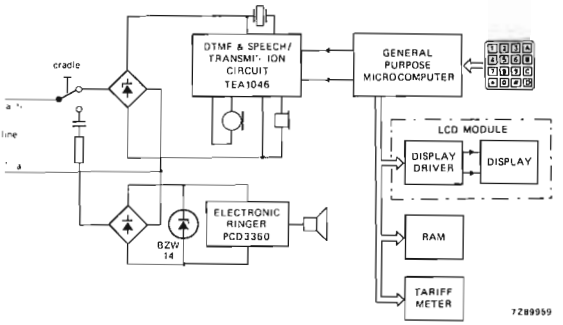
The PCD 3341 pulse repertory dialler/telephone-set-controller can store ten 16-digit numbers. It can also be augmented by connecting eight PCD 8571 CMOS RAMs to the I²C-bus (a two-wire serial I/O that can be used to connect peripherals to the PCD 3341).

Besides the serial RAM, an LCD driver, a clock/timer circuit and DTMF peripherals PCD 3312 and PCD 3311 are available (the latter intended to operate with 4 or 8 bit microcomputers with parallel interface).

Fig. 3b shows a variation using a general-purpose microcomputer with parallel I/O in conjunction with the TEA 1046 DTMF/speech/transmission IC (which has microcomputer compatible keyboard inputs).



(a) Feature-phone using dedicated microcomputer PCD334-1.



(b) Variation using a general-purpose microcomputer with parallel I/O.

Fig.3 Subscriber-set architecture with extended features.

COMPARISONS

Bipolar DTMF generators	TDA1077	TEA1021	TEA1043	TEA1044
I^2L technology	●	●	●	●
on-chip line adaption	●	●	●	●
mute output			●	●
adjustable dynamic impedance				●
crystal oscillator frequency (MHz)	4,78	4,78	4,78	4,78
min. line current (mA) max. or guaranteed	15	10	10	10
min. line current (mA) typical	12	8	8	8
number of pins	16	16	16	18
external filter components required to meet CEPT CS203 recommendation	2 R 2 C L (15 mH)	2 R 3 C	2 R 2 C L (15 mH)	2 R 3 C

Transmission ICs	TEA 1042	TEA 1053	TEA 1054	TEA 1055	TEA 1060	TEA 1061	TEA 1062	TEA 1063
microphone inputs								
low sensitivity – dynamic or magnetic					●		●	
medium sensitivity – dynamic or magnetic	●	●	●		●		●	
electret with source follower						●		●
electret with preamplifier	●			●		●		●
piezo-electric						●		●
electret with preamplifier (loudspeaker)	●							
receiver outputs								
dynamic or magnetic	●	●	●	●	●	●	●	●
piezo-electric					●	●	●	●
output for loudspeaker amplifier	●							
mode switch handset/loudspeaker	●							
electronic mute input	●	●	●	●	●	●		
DTMF input	●	●	●	●	●	●		
voltage regulator								
adjustable d.c. voltage	●	●	●	●				
adjustable d.c. resistance	●	●	●	●	●	●	●	●
power down input					●	●		
gain control								
control to be switched off	●	●	●	●	●	●	●	●
adapted to 400 Ω feed	●		●	●				
adapted to 600 Ω feed					●	●	●	●
adapted to 800 Ω feed	●	●		●				
adaptable to exchange sypply voltage	●	●	●	●	●	●	●	●

	PCD3320	PCD3321	PCD3332	PCD3323	PCD3324	PCD3325
number of pins	18	18	18	28	18	18
dial-pulse frequencies (Hz)	10	10	10	10	10	10
or		16		16	16	16
or		20		20	20	20
mark/space ratio	3/2	3/2	3/2	3/2	3/2	3/2
or		2/1		2/1	2/1	2/1
interdigit pause duration (ms)						
@ 10 Hz dial-pulse frequency	790	790	790	790	790	790
or				888		
@ 16 Hz dial-pulse frequency		515		515	515	515
or				579		
@ 20 Hz dial-pulse frequency		412		412	412	412
or				463		
reset delay for line power breaks (ms)						
@ 10 Hz dial-pulse frequency	158	158	158	158	158	158
or				316		
@ 16 Hz dial-pulse frequency		103		103	103	103
or				206		
@ 20 Hz dial-pulse frequency		82,4		82,4	82,4	82,4
or				165		
access-pause duration (s)						
@ 10 Hz dial-pulse frequency		3,16		3,16	3,16	1)
or				6,32		
@ 16 Hz dial-pulse frequency		2,06		2,06	2,06	1)
or				4,12		
@ 20 Hz dial-pulse frequency		1,65		1,65	1,65	1)
or				3,30		
max. number of automatically-inserted access pauses	0	2	0	2	1	0
manually-insertable access pauses		●		●	●	●
I/Os						
M1, mute output	●	●	●	●	●	●
$\overline{M1}$, inverted output	●		●	●		
M2, strobe output			●	●		
M3, M1·$\overline{DP}$	●			●		
CL, clock output				●		
APO, access pause output 2)		●		●	●	●
APR, access pause reset				●		
AAE, automatic access-pause enable				●		
* key recognition		●		●	●	●

1) terminated by access tone or via keyboard
2) connected to HOLD input in PCD 3321/3324/3325

BIPOLAR ICs FOR TELEPHONE SUBSCRIBER SETS

TWO-TONE GENERATOR FOR TELEPHONE DIALLING

This integrated circuit is a tone generator, supplying frequency combinations (in accordance with CCITT recommendations) for use in push-button telephones.

The various frequencies are derived from a crystal-controlled oscillator followed by a sine-wave synthesizer. I^2L technology is used, allowing the use of both digital and analogue functions. The built-in current/voltage regulator and output amplifier substantially reduce the number of external components. Only a quartz crystal of 4,783 MHz, a few resistors and capacitors are required. The circuit features:

- Stabilized working voltage.
- Frequency synthesizer.
- Adjustable output level.
- Output stage included.
- Two key roll-over provided.
- Keyboard inputs protected.

QUICK REFERENCE DATA

Working voltage	V_P	typ.	3,3 V
Supply current range	I_P		15 to 150 mA
Surge current (max. 100 μs)	I_S	max.	850 mA
Low frequencies	f		697, 770, 852 and 941 Hz
High frequencies	f		1209, 1336, 1477 and 1633 Hz
Operating ambient temperature	T_{amb}		−25 to + 70 °C
Storage temperature	T_{stg}		−55 to + 125 °C

PACKAGE OUTLINES

TDA1077P: 16-lead DIL; plastic (SOT-38).
TDA1077D: 16-lead DIL; ceramic (SOT-74).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Input series resistance	R_S	min.	33 Ω
Supply current	I_P	max.	150 mA
Surge current (max. 100 μs)	I_S	max.	850 mA
Operating ambient temperature	T_{amb}		−25 to + 70 °C
Storage temperature	T_{stg}		−55 to + 125 °C
Junction temperature	T_j	max.	125 °C

CHARACTERISTICS

Working voltage (d.c.)			
I_O = 15 mA; T_{amb} = 25 °C	V_P	typ.	3,3 V
		<	3,8 V
Supply current			
TDA1077P	I_P		15 to 80 mA
TDA1077D	I_P		15 to 120 mA
Low frequencies	f		697, 770, 852 and 941 Hz
High frequencies	f		1209, 1336, 1477 and 1633 Hz
Frequency accuracy		typ.	0,2 %*
		<	1,5 %
Nominal output (adjustable by R3; see Figs 1 and 2)			
Lower tones			−6 to −11 dBm
Higher tones			−4 to −9 dBm
Tolerance on total output level			± 2 dB
Pre-emphasis			1,2 to 2,5 dB
		typ.	2 dB
Maximum total distortion with respect to total level	d_{tot}	<	−24 dB
		<	−30 dB*
Unwanted signal levels			
< 3,4 kHz		<	−33 dBm
< 3,4 kHz		typ.	−40 dBm*
> 50 kHz		typ.	−80 dBm*
Tone delay after actuation	t_d	<	7 ms*
Switch bounce elimination	t_{sb}	typ.	1 ms
Keyboard resistance			
Contact "ON"	R_{Kon}	<	10 kΩ
Contact "OFF"	R_{Koff}	>	300 kΩ

* Values with recommended external components; see Figs 1 and 2.

APPLICATION INFORMATION

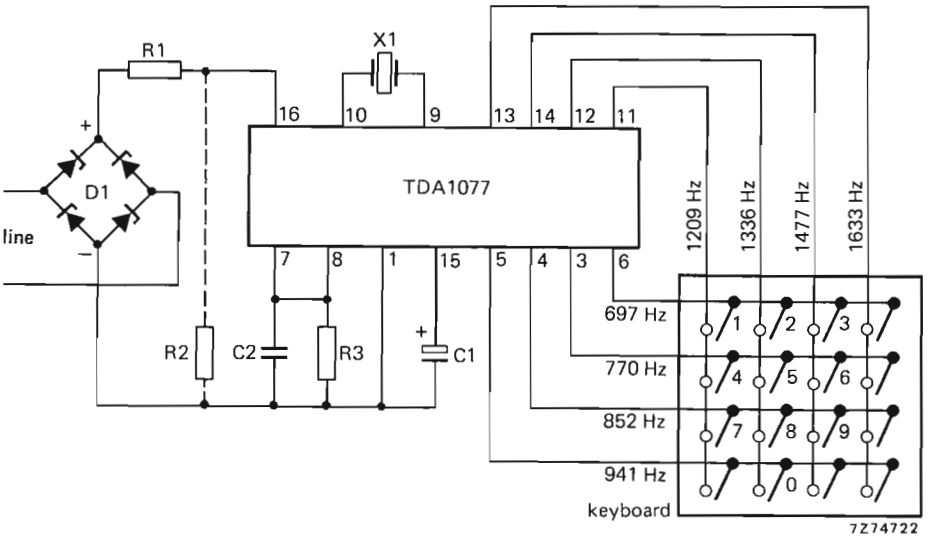


Fig. 1 Circuit diagram for telephone tone generator.

Internal resistance R_i = 900 Ω when R2 = ∞.
Internal resistance R_i = 600 Ω when R2 = 1500 Ω.
R3 adjusts tone output level; exact value depends on load impedance and required output level.

Components

R1 metal film resistor MR25 5%	33 Ω
R2 metal film resistor MR25 5%	1500 Ω
R3 metal film resistor MR24	≈ 2 kΩ
C1 solid Al. electrolytic 6,3 V	4,7 μF
C2 met. pol. film cap. 10% (nugget)	27 nF
D1 transient suppressor bridge	BZW10
X1 quartz crystal	4,783 MHz

APPLICATION INFORMATION (continued)

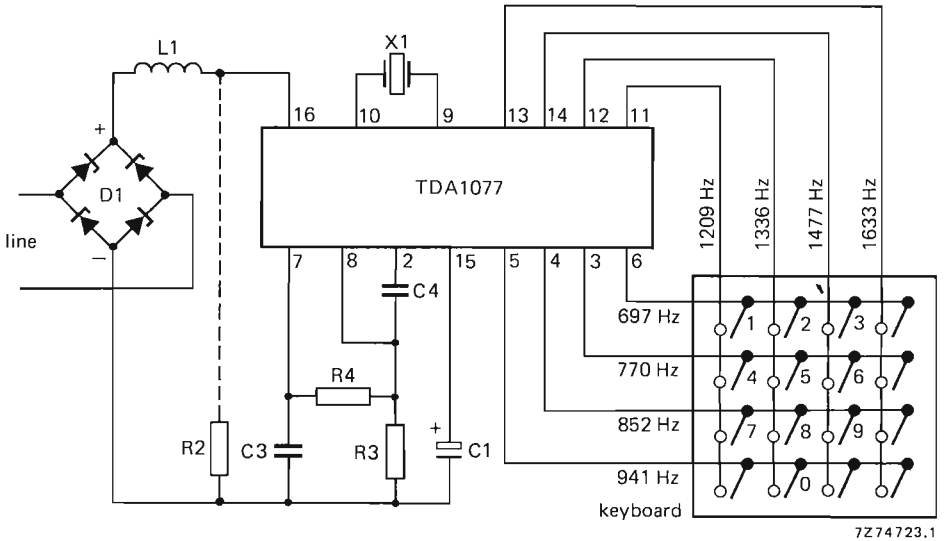


Fig. 2 Circuit diagram for telephone tone generators including C.I.S.P.R. requirements. Low harmonic distortion (–80 dBm at 50 kHz).

Components

R2 metal film resistor MR25 5%	1500 Ω	C1 solid Al. electrolytic 6,3 V	4,7 μF
R3 metal film resistor MR24	≈ 2 kΩ	C3 miniature ceramic plate cap. 2%	10 nF
R4 metal film resistor MR24 1%	4,7 kΩ	C4 met. pol. film cap. 10%	33 nF
L1 coil (33 Ω)	15 mH	D1 transient suppressor bridge	BZW10
		X1 quartz crystal	4,783 MHz

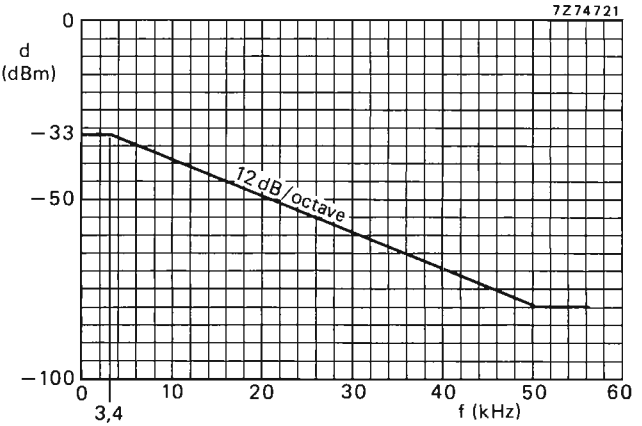
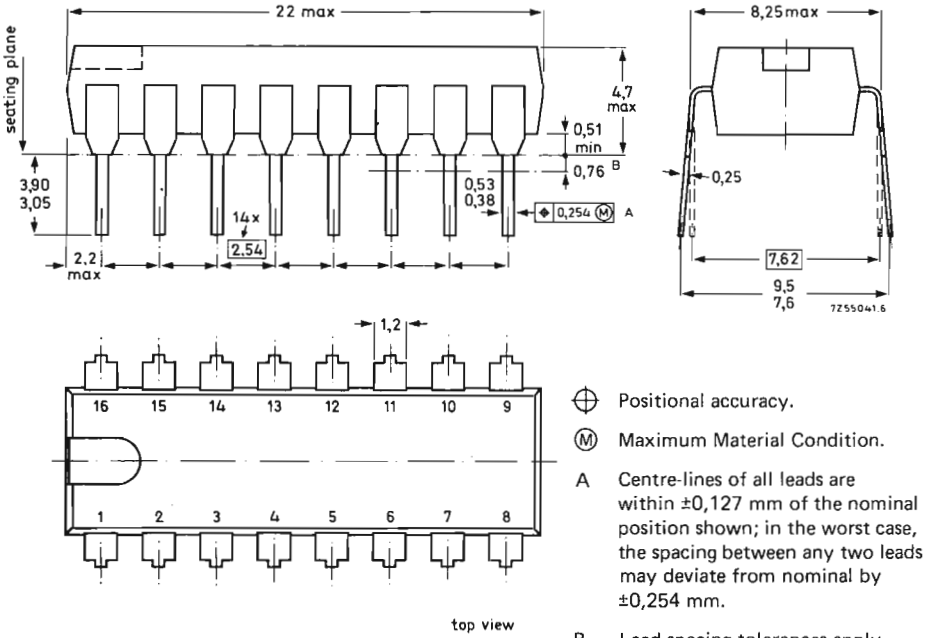


Fig. 3 Harmonic distortion.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

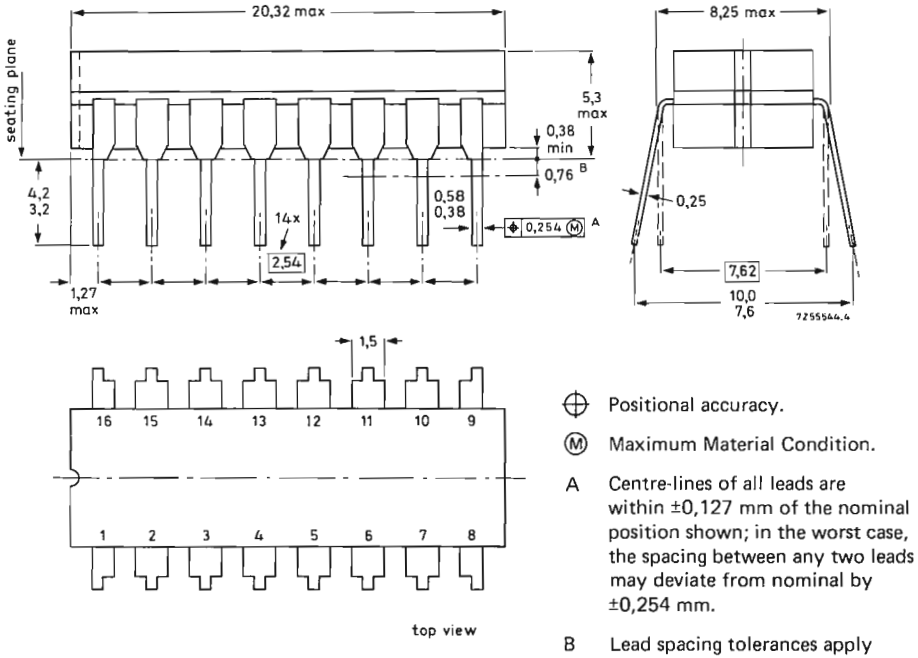
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; CERAMIC (SOT-74)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

DTMF GENERATOR FOR TELEPHONE DIALLING

This integrated circuit is a dual-tone multi-frequency (DTMF) generator, supplying frequency combinations (in accordance with CCITT recommendations) for use in pushbutton telephones, with a common contact on the keyboard for muting.

The various frequencies are derived from a crystal-controlled oscillator followed by a sinewave synthesizer.

I^2L technology allows digital and analogue functions to be implemented on the same chip. The built-in current/voltage regulator and active output amplifier substantially reduce the number of external components. Only a quartz crystal of 4,78 MHz and a few resistors and capacitors are required.

The circuit features:
- wide operating line current range
- operating voltage down to 1,3 volt
- no individual tone level adjustment required
- temperature stabilized signal levels
- line current independent signal levels
- output stage and line regulator included
- all pins protected against electrostatic discharges
- two key roll-over provided
- operates with a low cost quartz crystal
- few external components required

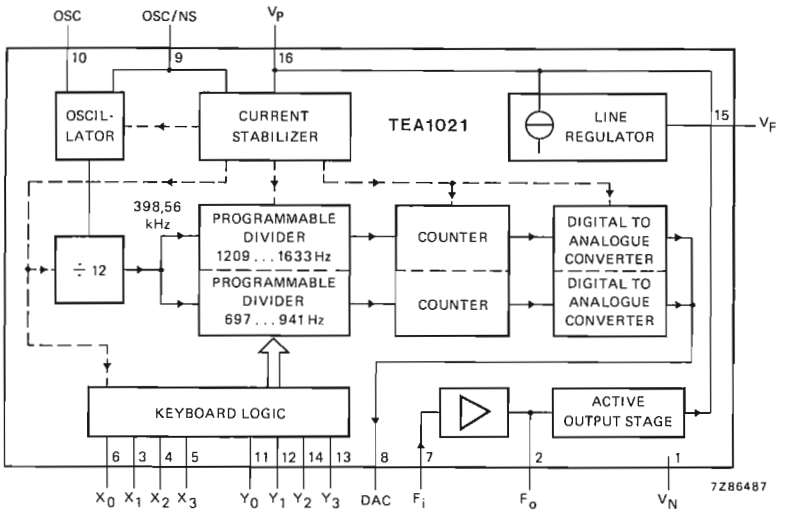


Fig. 1 Block diagram (dotted lines are stabilized supply rails).

PACKAGE OUTLINES

TEA1021P: 16-lead DIL, plastic (SOT-38).
TEA1021D: 16-lead DIL, ceramic (SOT-74B).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150	mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	850	mA
Input series resistance	R_s	min.	18	Ω
Operating ambient temperature range	T_{amb}	−25 to	+ 70	°C
Storage temperature range	T_{stg}	−55 to	+ 125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS

V_N = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit	conditions
operating voltage						
d.c.; $-I_L$ = 10 mA	V_L	2,8	3,3	3,8	V	
line current						
level − 7 dBm	I_L	10	8	120	mA	
level − 2 dBm	I_L	12	9	120	mA	
internal impedance	Z_i	640	900	1150	Ω	300 − 3400 Hz
tone frequencies						
low	f_{x0}	−	697	−	Hz	frequency quartz crystal 4 782 720 Hz
	f_{x1}	−	770	−	Hz	
	f_{x2}	−	852	−	Hz	
	f_{x3}	−	941	−	Hz	
high	f_{y0}	−	1209	−	Hz	
	f_{y1}	−	1336	−	Hz	
	f_{y2}	−	1477	−	Hz	
	f_{y3}	−	1633	−	Hz	
dividing error		−	−	0,11	%	
nom. output level						
lower frequency	V_{LG}	−	−	−6	dBm	adjustable
higher frequency	V_{HG}	−	−	−4	dBm	adjustable
tolerance						
on output level	ΔV_o	2	−	2	dB	
pre-emphasis		1,3	2	2,7	dB	without filter components
distortion with respect to total level	d_{tot}	−	−34	−24	dB	maximum tone level and with first-order filter
start up time	t_s	−	5	−	ms	with recommended external components
switch bounce elimination	t_{sb}	1	1,5	2	ms	
required keyboard resistance						
contact on	$R_{k\ on}$	−	−	10	kΩ	
contact off	$R_{k\ off}$	500	−	−	kΩ	

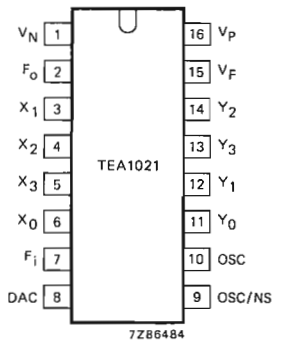


Fig. 2 Pin designation.

PINNING

1	V_N	negative supply
2	F_o	filter output
3	X1	row keyboard input 1
4	X2	row keyboard input 2
5	X3	row keyboard input 3
6	X0	row keyboard input 0
7	F_i	filter input/input audio amplifier
8	DAC	output DAC/DTMF tones
9	OSC/NS	oscillator/noise suppression output
10	OSC	oscillator input
11	Y0	column keyboard input 0
12	Y1	column keyboard input 1
13	Y3	column keyboard input 3
14	Y2	column keyboard input 2
15	V_F	input low-pass filter
16	V_P	positive supply

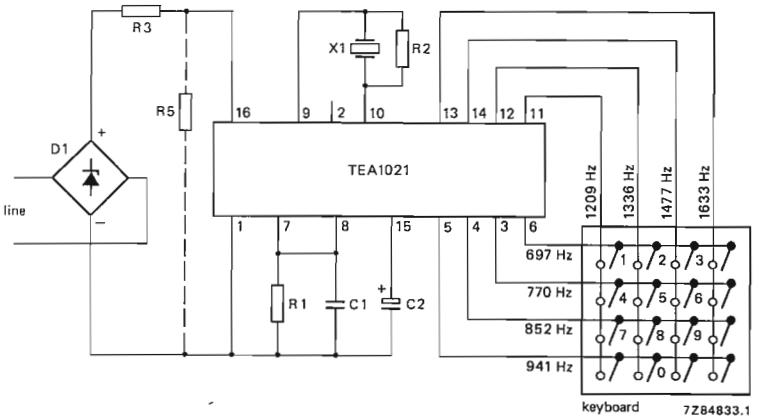


Fig. 3 Application diagram with first-order filter.

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	18 Ω
R5	metal film resistor	SFR16	5%	2700 Ω (for Z_o = 600 Ω; no resistor for Z_o = 900 Ω)
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
D1	polarity guard and transient suppressor bridge (see Fig. 6)			2 x BAS11 and 2 x BZW03-..
X1	quartz crystal			4,783 MHz

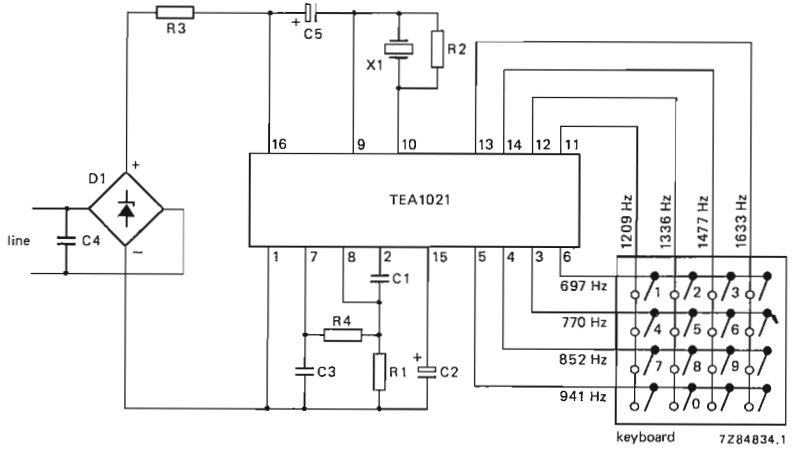


Fig. 4 Application diagram with second-order filter to minimize harmonic distortion (meets CEPT CS203 requirements).

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	18 Ω
R4	metal film resistor	SFR16	5%	270 kΩ
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
C3	miniature ceramic plate capacitor			180 pF
C4	metallized polyester film capacitor			22 nF
C5	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
D1	transient suppressor bridge (see Fig. 6)			2 x BAS11 and 2 x BZW03-..
X1	quartz crystal			4,783 MHz

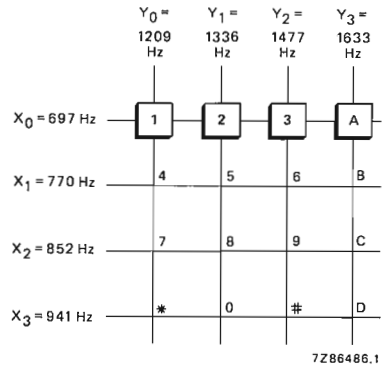


Fig. 5 Allocation of dialling tones to keyboard functions.

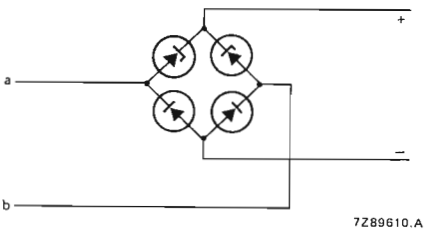


Fig. 6 Polarity-guard and line-transient suppression bridge D1.
Diodes 2 x BAS11.
Voltage regulators 2 x BZW03-..

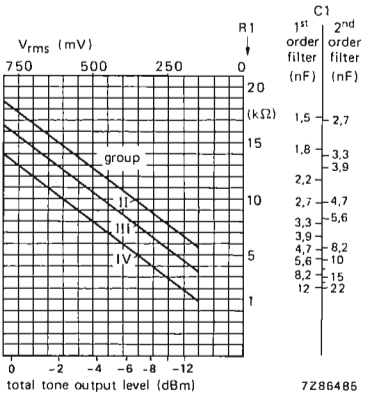


Fig. 7 Level adjustment (see Figs 3 and 4).

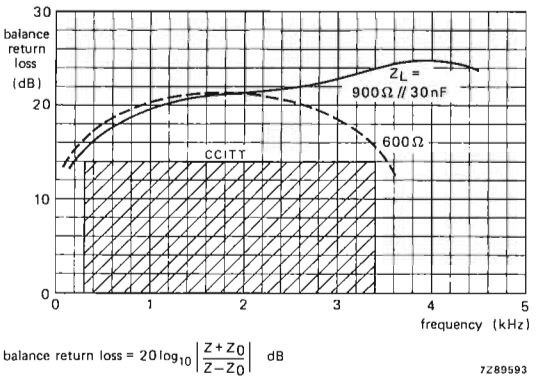


Fig. 8 Balance return loss measured with external components as in Fig. 4.

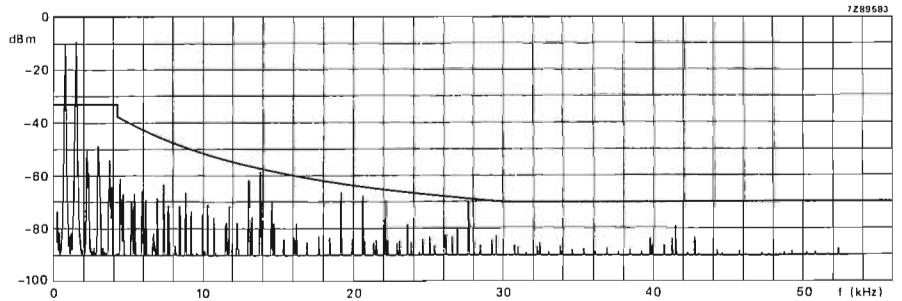


Fig. 9 Frequency spectrum of circuit with second-order filter (see Fig. 4).

APPLICATION (see Fig. 4)

Line matching

If there is an impedance match between the lines and the dialling circuit, the balance return loss will be high and reflections on the line will be highly damped. Figure 8 shows that the balance return loss when using the application diagram as shown in Fig. 4 is more than 14 dB. The variation of balance return loss with the frequency is largely caused by an impedance variation due to the low-pass filter capacitor (C2) and the radio-frequency interference filter capacitor C4. Since the highest line impedance that is likely to be encountered is 900 Ω the internal impedance of the dialling circuit is set at this level and can be reduced to match lower impedance lines by adding an external resistor between pins 1 and 16. If direct current must be eliminated a capacitor must be connected in series with the resistor.

– internal impedance Z_i = 900 Ω; no external resistor between pins 1 and 16.
– internal impedance Z_i = 600 Ω; external resistor between pins 1 and 16 = 2700 Ω.

Output level adjustment

The tone output levels are subject to some spread due to manufacturing tolerances and can be adjusted by selection of the value of the resistor connected to pin 8.
The level of the higher-frequency tone however is always 2 ± 0,7 dB above that of the lower-frequency tone. The total production of the circuits is therefore divided into groups. The group to which any of the integrated circuits belongs is identified by dots on the body of the circuit, the number of dots corresponding with the group number. The combined tone output level is shown as a function of resistor value with group number as a parameter in Fig. 7. After the resistor value has been selected to obtain the required tone output level, the value of the filter capacitor connected to the same pin must be determined. For passive first-order filters (Fig. 4) the time-constant (RC) must be 26 μs. For active second-order filters it must be 46 μs. These values accommodate the different attenuation levels for the various tone frequencies due to the 0,3 dB hump at the breakpoint of the filters.

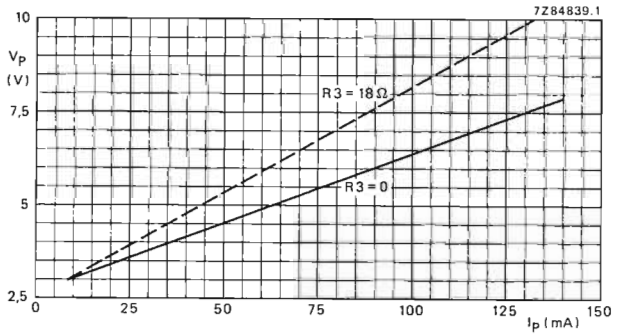
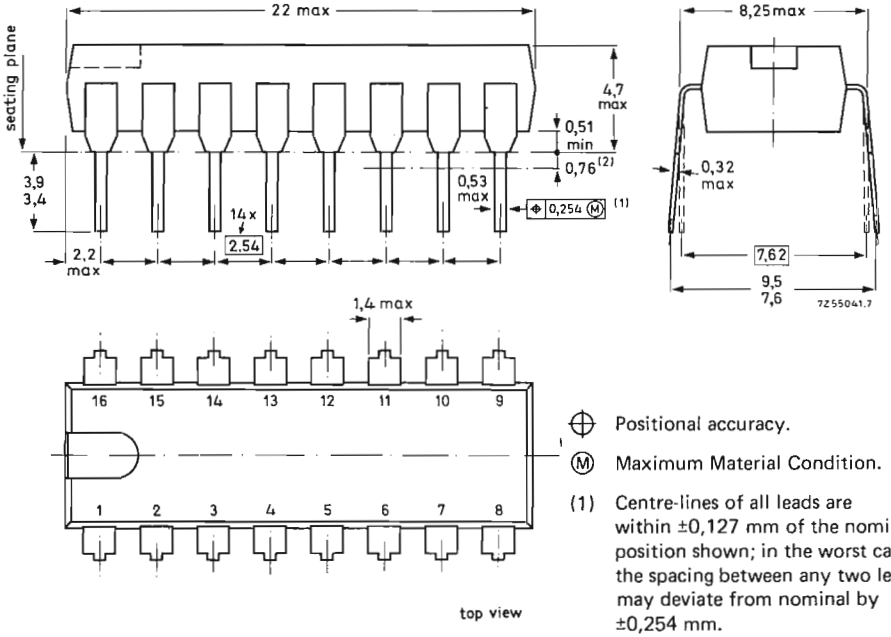


Fig. 10 D.C. characteristics.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

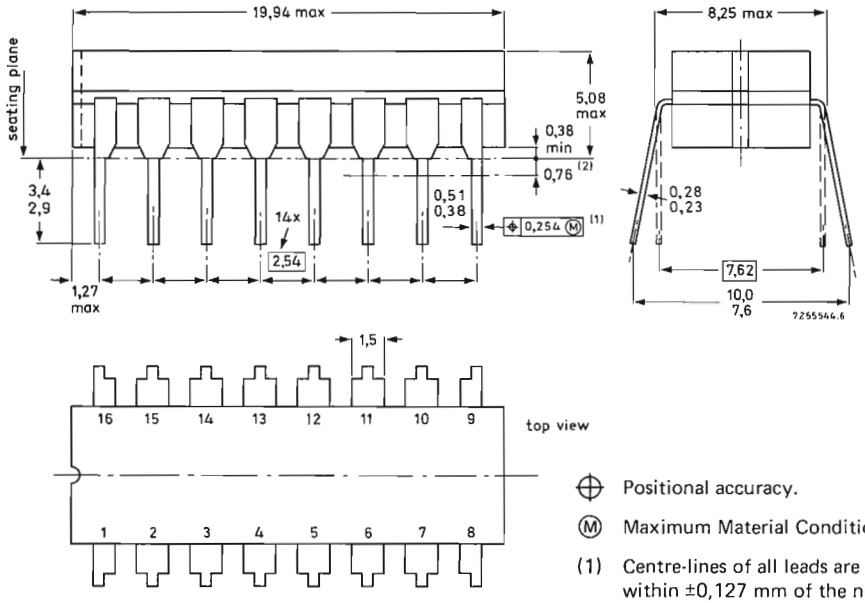
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; CERAMIC (SOT-74)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

DTMF GENERATOR FOR TELEPHONE DIALLING

This integrated circuit is a dual-tone multi-frequency (DTMF) generator, supplying frequency combinations (in accordance with CCITT recommendations) for use in pushbutton telephones, with a single contact keyboard.

The various frequencies are derived from a crystal-controlled oscillator followed by a sinewave synthesizer.

I^2L technology allows digital and analogue functions to be implemented on the same chip. The built in current/voltage regulator and active output amplifier substantially reduce the number of external components. Only a quartz crystal of 4,78 MHz and a few resistors and capacitors are required.

The circuit features:
- wide operating line current range
- operating voltage down to 1,3 volt (standby 0,7 volt)
- no individual tone level adjustment required
- temperature stabilized signal levels
- line current independent signal levels
- output stage and line regulator included
- all pins protected against electrostatic discharges
- two key roll-over provided
- operates with a low cost quartz crystal
- few external components required
- electronic mute facility
- low power consumption in standby mode

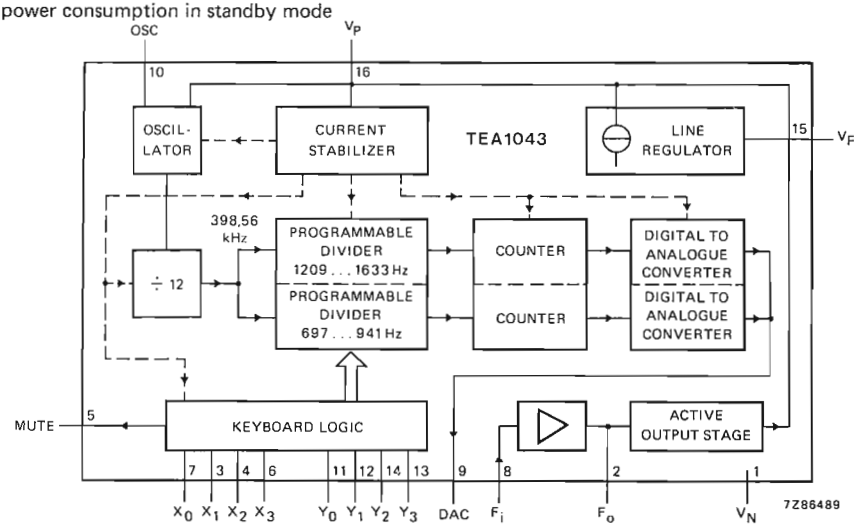


Fig. 1 Block diagram (dotted lines are stabilized supply rails).

PACKAGE OUTLINES

TEA1043P: 16-lead DIL, plastic (SOT-38).
TEA1043D: 16-lead DIL, ceramic (SOT-74B).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150	mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	850	mA
Input series resistance	R_s	min.	18	Ω
Operating ambient temperature range	T_{amb}		−25 to +70	°C
Storage temperature range	T_{stg}		−55 to +125	°C
Junction temperature	T_j	max.	125	°C

CHARACTERISTICS

$V_N = 0$ V; $T_{amb} = -25$ to +70 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit	conditions
operating voltage						
d.c.; $-I_L = 10$ mA	V_L	2,8	3,3	3,8	V	
line current						
level − 7 dBm	I_L	10	8	120	mA	
level − 2 dBm	I_L	12	9	120	mA	
standby mode	I_L	–	50	–	μA	
internal impedance	Z_i	640	900	1150	Ω	300 − 3400 Hz
tone frequencies						
low	f_{x0}	–	697	–	Hz	
	f_{x1}	–	770	–	Hz	
	f_{x2}	–	852	–	Hz	frequency
	f_{x3}	–	941	–	Hz	quartz crystal 4 782 720 Hz
high	f_{y0}	–	1209	–	Hz	
	f_{y1}	–	1336	–	Hz	
	f_{y2}	–	1477	–	Hz	
	f_{y3}	–	1633	–	Hz	
dividing error		–	–	0,11	%	
nom. output level						
lower freq.	V_{LG}	–	–	−6	dBm	adjustable
higher freq.	V_{HG}	–	–	−4	dBm	adjustable
tolerance on output level	ΔV_o	2	–	2	dB	
pre-emphasis		1,3	2	2,7	dB	without filter components
distortion with respect to total level	d_{tot}	–	−34	−24	dB	maximum tone level and with first-order filter
start up time	t_s	–	5	–	ms	with recommended external components
mute output sink current	I_{MS}	–	–	0,5	mA	
switch bounce elimination	t_{sb}	1	1,5	2	ms	
required keyboard resistance						
contact on	$R_{k\ on}$	–	–	10	kΩ	
contact off	$R_{k\ off}$	500	–	–	kΩ	

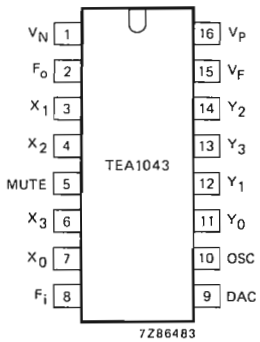


Fig. 2 Pin designation.

PINNING

1	V_N	negative supply
2	F_o	filter output
3	X1	row keyboard input 1
4	X2	row keyboard input 2
5	MUTE	mute output
6	X3	row keyboard input 3
7	X0	row keyboard input 0
8	F_i	filter input/ input audio amplifier
9	DAC	output DAC/DTMF tones
10	OSC	oscillator input
11	Y0	column keyboard input 0
12	Y1	column keyboard input 1
13	Y3	column keyboard input 3
14	Y2	column keyboard input 2
15	V_F	input low-pass filter
16	V_P	positive supply

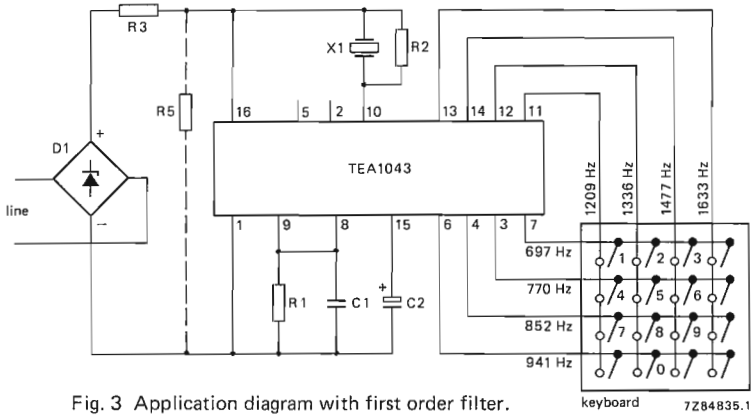


Fig. 3 Application diagram with first order filter.

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	18 Ω
R5	metal film resistor	SFR16	5%	2700 Ω (for Z_o = 600 Ω; no resistor for Z_o = 900 Ω)
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitors		6,3 V	4,7 μF
D1	polarity guard and transient suppressor bridge (see Fig. 6)			2 x BAS11 and 2 x BZW03–..
X1	quartz crystal			4, 783 MHz

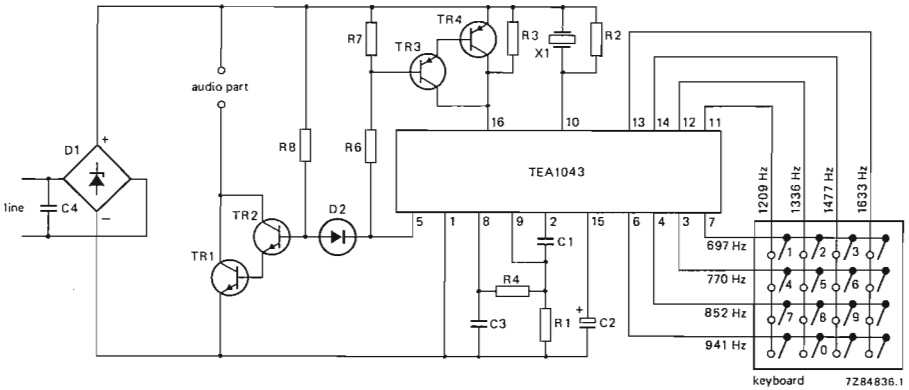


Fig. 4 Application diagram with electronic mute switch and second-order filter.

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	39 kΩ (depends on audio voltage)
R4	metal film resistor	SFR16	5%	270 kΩ
R6	metal film resistor	SFR16	5%	330 kΩ
R7	metal film resistor	SFR16	5%	820 kΩ
R8	metal film resistor	SFR16	5%	470 kΩ
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
C3	miniature ceramic plate capacitor			180 pF
C4	metallized polyester film capacitor			22 nF
D1	transient suppressor bridge (see Fig. 6)	2 x BAS11 and 2 x BZW03–..		
D2	diode	BAW62		
TR1	transistor	BC338		
TR2	transistor	BC548		
TR3	transistor	BC558		
TR4	transistor	BC328		
X1	quartz crystal			4,783 MHz

If TR1/TR2 = BSR50 and TR3/TR4 = BSR60 then R6 = 39 kΩ, R7 = 120 kΩ and R8 = 33 kΩ.

An additional choke of 15 mH in series with the circuit is required to meet the CEPT CS203 distortion requirements.

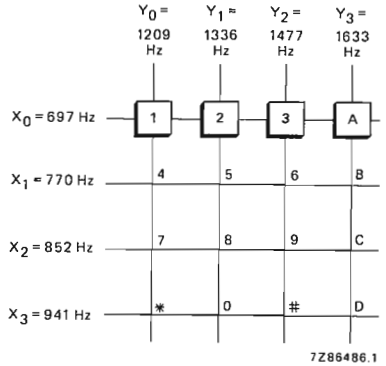


Fig. 5 Allocation of dialling tones to keyboard functions.

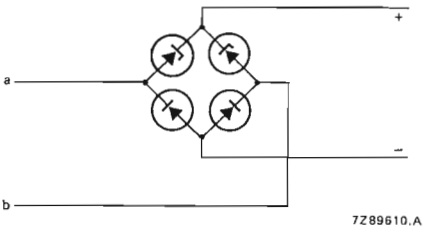


Fig. 6 Polarity-guard and line-transient suppression bridge D1. Diodes 2 x BAS11. Voltage regulators 2 x BZW03−..

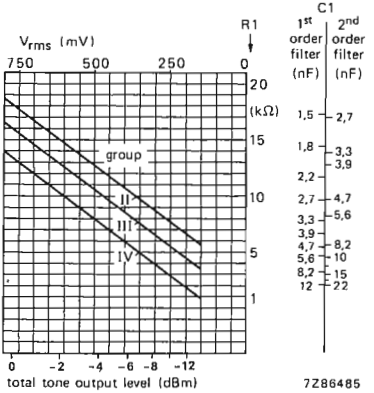


Fig. 7 Level adjustment (see Figs 3 and 4).

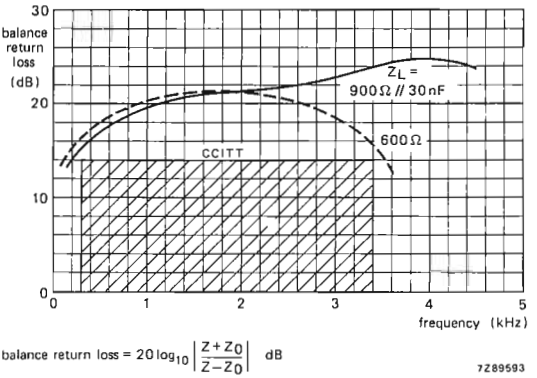


Fig. 8 Balance return loss measured with external components as in Fig. 4.

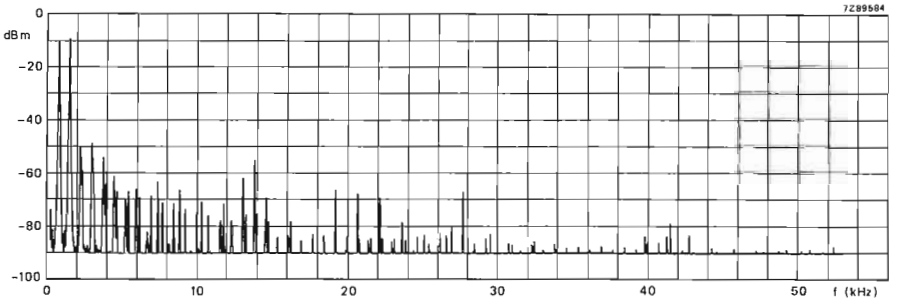


Fig. 9 Frequency spectrum of circuit with second order filter (see Fig. 4).

APPLICATION (see Fig. 4)

Line matching

If there is an impedance match between the lines and the dialling circuit, the balance return loss will be high and reflections on the line will be highly damped. Figure 8 shows that the balance return loss when using the application diagram as shown in Fig. 4 is more than 14 dB. The variation of balance return loss with the frequency is largely caused by an impedance variation due to the low-pass filter capacitor (C2) and the radio-frequency interference filter capacitor C4. Since the highest line impedance that is likely to be encountered is 900 Ω the internal impedance of the dialling circuit is set at this level and can be reduced to match lower impedance lines by adding an external resistor between pins 1 and 16. If direct current must be eliminated a capacitor must be connected in series with the resistor.

– internal impedance Z_i = 900 Ω; no external resistor between pins 1 and 16.
– internal impedance Z_i = 600 Ω; external resistor between pins 1 and 16 = 2700 Ω.

Output level adjustment

The tone output levels are subject to some spread due to manufacturing tolerances and can be adjusted by selection of the value of the resistor connected to pin 8.
The level of the higher-frequency tone however is always 2 ± 0,7 dB above that of the lower-frequency tone. The total production of the circuits is therefore divided into groups. The group to which any of the integrated circuits belongs is identified by dots on the body of the circuit, the number of dots corresponding with the group number. The combined tone output level is shown as a function of resistor value with group number as a parameter in Fig. 7. After the resistor value has been selected to obtain the required tone output level, the value of the filter capacitor connected to the same pin must be determined. For passive first-order filters (Fig. 4) the time-constant (RC) must be 26 μs. For active second-order filters it must be 46 μs. These values accommodate the different attenuation levels for the various tone frequencies due to the 0,3 dB hump at the breakpoint of the filters.

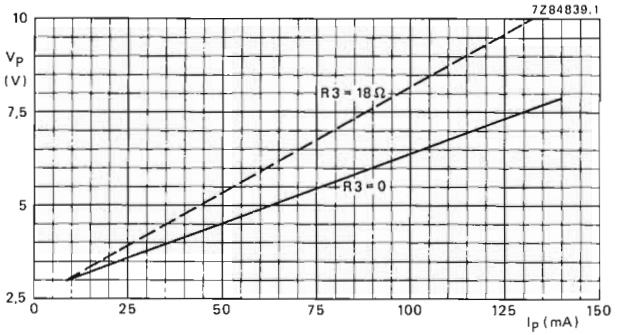
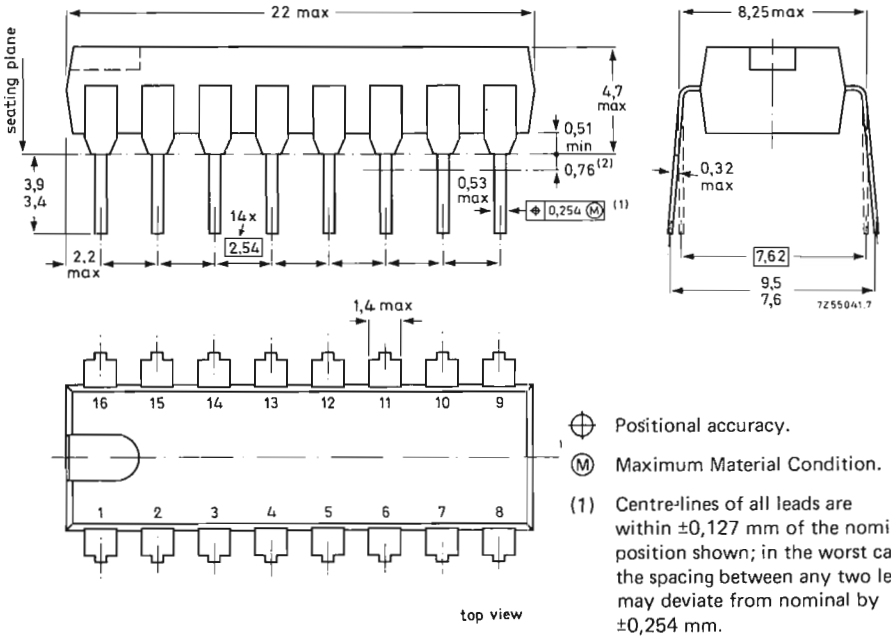


Fig. 10 D.C. characteristics.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

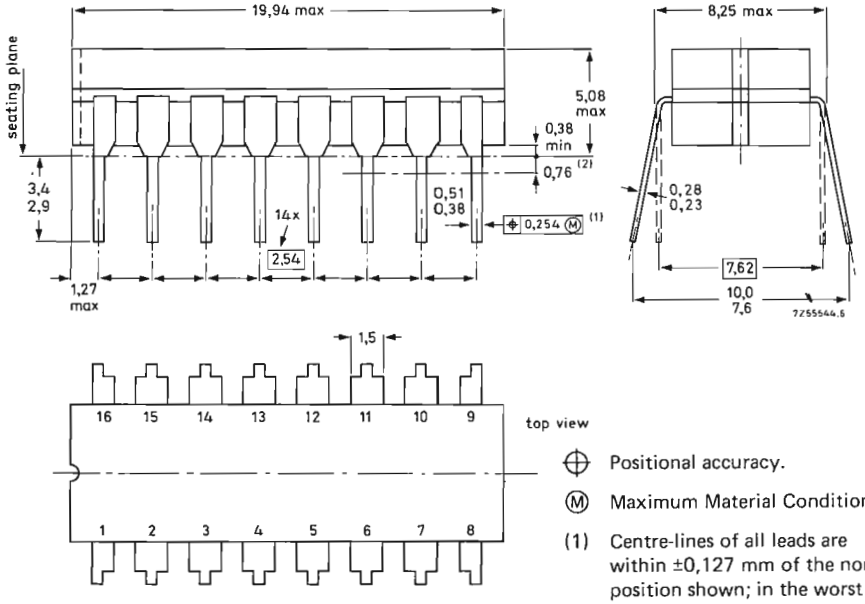
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; CERAMIC (SOT-74)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

DTMF GENERATOR FOR TELEPHONE DIALLING

This integrated circuit is a dual-tone multi-frequency (DTMF) generator, supplying frequency combinations (in accordance with CCITT recommendations) for use in pushbutton telephones, with a single contact keyboard.

The various frequencies are derived from a crystal-controlled oscillator followed by a sinewave synthesizer.

I^2L technology allows digital and analogue functions to be implemented on the same chip. The built in current/voltage regulator and active output amplifier substantially reduce the number of external components. Only a quartz crystal of 4,78 MHz and a few resistors and capacitors are required.

The circuit features:
- wide operating line current range
- operating voltage down to 1,3 volt (standby 0,7 volt)
- no individual tone level adjustment required
- temperature stabilized signal levels
- line current independent signal levels
- output stage and line regulator included
- all pins protected against electrostatic discharges
- two key roll-over provided
- operates with a low cost quartz crystal
- few external components required
- electronic mute facility
- adjustable impedance
- low power consumption in standby mode

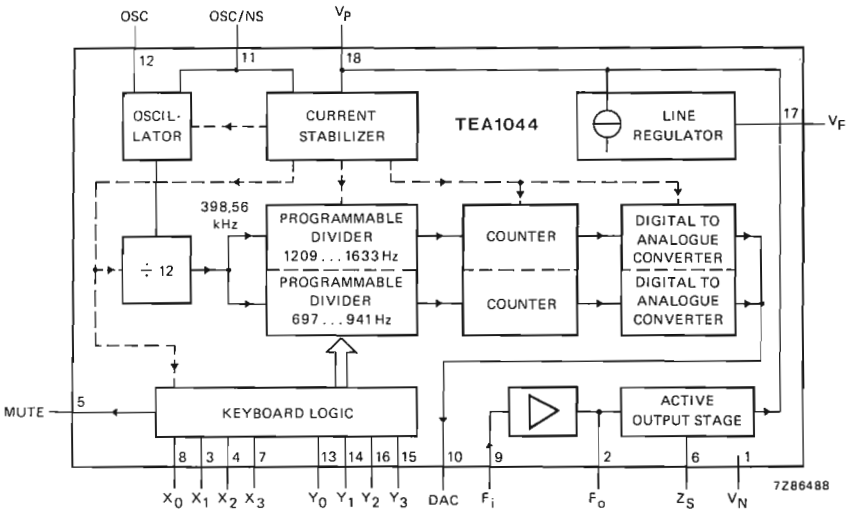


Fig. 1 Block diagram (dotted lines are stabilized supply rails).

PACKAGE OUTLINES

TEA1044P : 18-lead DIL, plastic (SOT-102A).
TEA1044D: 18-lead DIL, ceramic (SOT-133).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150 mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	850 mA
Input series resistance	R_s	min.	18 Ω
Operating ambient temperature range	T_{amb}	−25 to	+70 °C
Storage temperature range	T_{stg}	−55 to	+125 °C
Junction temperature	T_j	max.	125 °C

CHARACTERISTICS

V_N = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit	conditions
operating voltage d.c.; $-I_L$ = 10 mA	V_L	2,8	3,3	3,8	V	
line current						
level − 7 dBm	I_L	10	8	120	mA	
level − 2 dBm	I_L	12	9	120	mA	
standby current	I_{LS}	–	50	–	μA	
internal impedance	Z_i	640	900	1150	Ω	300 – 3400 Hz
tone frequencies						
low	f_{x0}	–	697	–	Hz	frequency quartz crystal 4 782 720 Hz
	f_{x1}	–	770	–	Hz	
	f_{x2}	–	852	–	Hz	
	f_{x3}	–	941	–	Hz	
high	f_{y0}	–	1209	–	Hz	
	f_{y1}	–	1336	–	Hz	
	f_{y2}	–	1477	–	Hz	
	f_{y3}	–	1633	–	Hz	
dividing error		–	–	0,11	%	
nom. output level						
lower frequency	V_{LG}	–	–	−6	dBm	adjustable
higher frequency	V_{HG}	–	–	−4	dBm	adjustable
tolerance on output level	ΔV_o	2	–	2	dB	
pre-emphasis		1,3	2	2,7	dB	without filter components
distortion with respect to total level	d_{tot}	–	−34	−24	dB	maximum tone level and with first-order filter
start up time	t_s	–	5	–	ms	with recommended external components
mute output sink current	I_{MS}	–	–	0,5	mA	
switch bounce elimination	t_{sb}	1	1,5	2	ms	
required keyboard resistance						
contact on	$R_{k\ on}$	–	–	10	kΩ	
contact off	$R_{k\ off}$	500	–	–	kΩ	

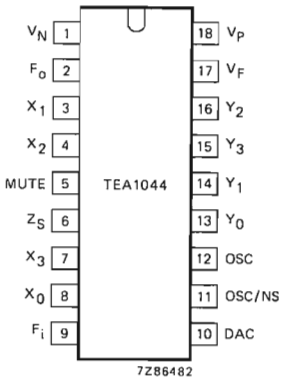


Fig. 2 Pin designation.

PINNING

1	V_N	negative supply
2	F_o	filter output
3	X1	row keyboard input 1
4	X2	row keyboard input 2
5	MUTE	mute output
6	Z_S	impedance setting
7	X3	row keyboard input 3
8	X0	row keyboard input 0
9	F_i	filter input/input audio amplifier
10	DAC	output DAC/DTMF tones
11	OSC/NS	oscillator/noise suppression output
12	OSC	oscillator input
13	Y0	column keyboard input 0
14	Y1	column keyboard input 1
15	Y3	column keyboard input 3
16	Y2	column keyboard input 2
17	V_F	input low-pass filter
18	V_P	positive supply

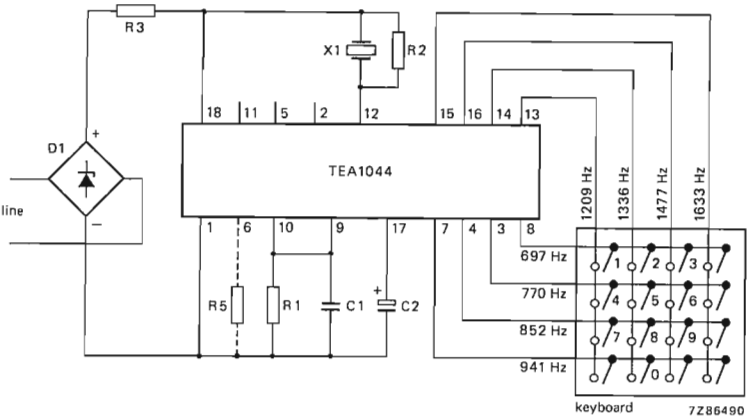


Fig. 3 Application diagram with first-order filter.

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	18 Ω
R5	metal film resistor	SFR16	5%	240 Ω (for Z_o = 600 Ω) no resistor for Z_o = 900 Ω
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
D1	polarity quard and transient suppressor bridge (see Fig. 6)			2 x BAS11 and 2 x BZW03-..
X1	quartz crystal			4,783 MHz

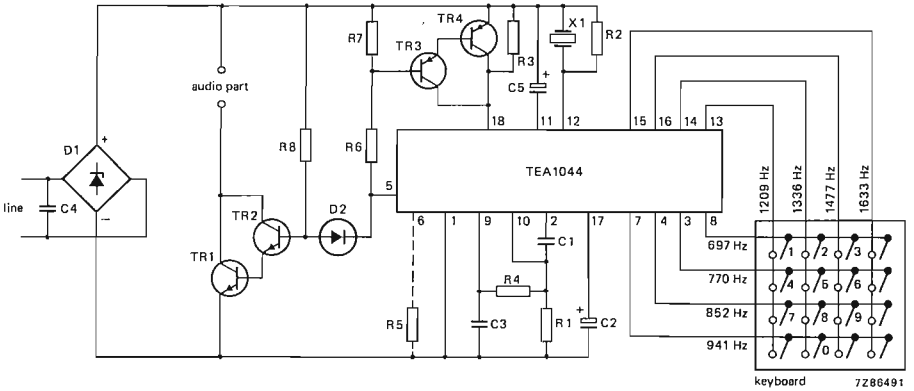


Fig. 4 Application diagram with electronic mute switch and second-order filter (meets CEPT CS203 requirements).

R1	metal film resistor	MR16	1%	see Fig. 7
R2	metal film resistor	SFR16	5%	3,3 MΩ
R3	metal film resistor	SFR16	5%	39 kΩ (depends on audio voltage)
R4	metal film resistor	SFR16	5%	270 kΩ
R5	metal film resistor	SFR16	5%	240 Ω (for Z_o = 600 Ω; no resistor for Z_o = 900 Ω)
C1	metallized polyester film capacitor			see Fig. 7
C2	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
C3	miniature ceramic plate capacitor			180 pF
C4	metallized polyester film capacitor			22 nF
C5	solid aluminium electrolytic capacitor		6,3 V	4,7 μF
D1	transient suppressor bridge (see Fig. 6)			2 x BAS11 and 2 x BZW03-..
D2	diode	BAW62		
TR1/TR2	transistors	BC338/BC548		
TR3/TR4	transistors	BC558/BC328		
X1	quartz crystal			4,783 MHz

If TR1/TR2 = BSR50 and TR3/TR4 = BSR60 then R6 = 39 kΩ, R7 = 120 kΩ and R8 = 33 kΩ

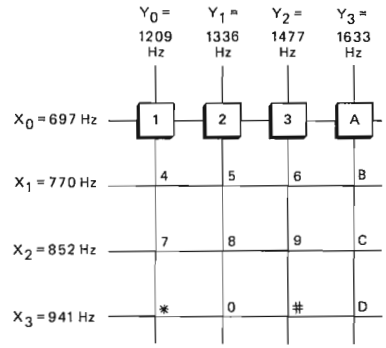


Fig. 5 Allocation of dialling tones to keyboard functions.

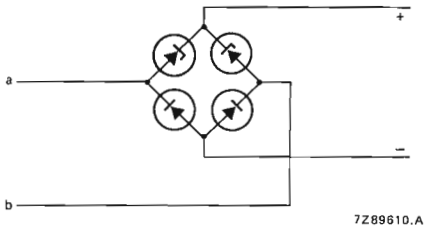


Fig. 6 Polarity-guard and line-transient suppression bridge D1. Diodes 2 x BAS11. Voltage regulators 2 x BZW03-..

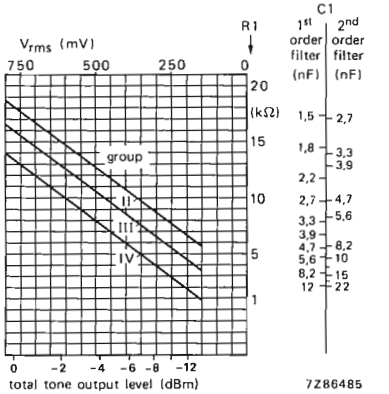


Fig. 7 Level adjustment (see Figs 3 and 4).

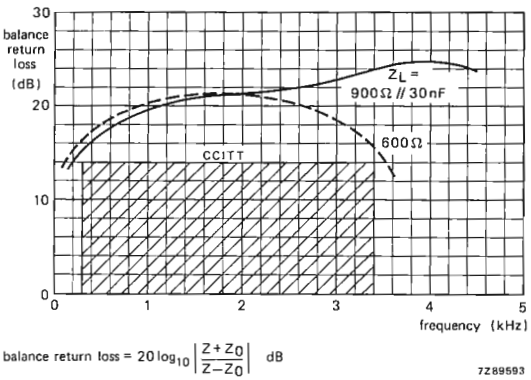


Fig. 8 Balance return loss measured with external components as in Fig. 4.

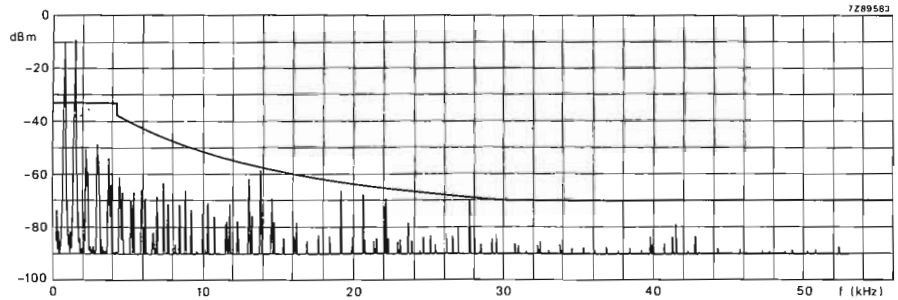


Fig. 9 Frequency spectrum of circuit with second-order filter (see Fig. 4).

APPLICATION (see Fig. 4)

Line matching

If there is an impedance match between the lines and the dialling circuit, the balance return loss will be high and reflections on the line will be highly damped. Figure 8 shows that the balance return loss when using the application diagram as shown in Fig. 4 is more than 14 dB. The variation of balance return loss with the frequency is largely caused by an impedance variation due to the low-pass filter capacitor (C2) and the radio-frequency interference filter capacitor C4. Since the highest line impedance that is likely to be encountered is 900 Ω the internal impedance of the dialling circuit is set at this level and can be reduced to match lower impedance lines by adding an external resistor between pins 1 and 6.

– internal impedance Z_i = 900 Ω; no external resistor between pins 1 and 6.
– internal impedance Z_i = 600 Ω; external resistor between pins 1 and 6 = 240 Ω.

Output level adjustment

The tone output levels are subject to some spread due to manufacturing tolerances and can be adjusted by selection of the value of the resistor connected to pin 8.
The level of the higher-frequency tone however is always 2 ± 0,7 dB above that of the lower-frequency tone. The total production of the circuits is therefore divided into groups. The group to which any of the integrated circuits belongs is identified by dots on the body of the circuit, the number of dots corresponding with the group number. The combined tone output level is shown as a function of resistor value with group number as a parameter in Fig. 7. After the resistor value has been selected to obtain the required tone output level, the value of the filter capacitor connected to the same pin must be determined. For passive first-order filters (Fig. 4) the time-constant (RC) must be 26 μs. For active second-order filters it must be 46 μs. These values accommodate the different attenuation levels for the various tone frequencies due to the 0,3 dB hump at the breakpoint of the filters.

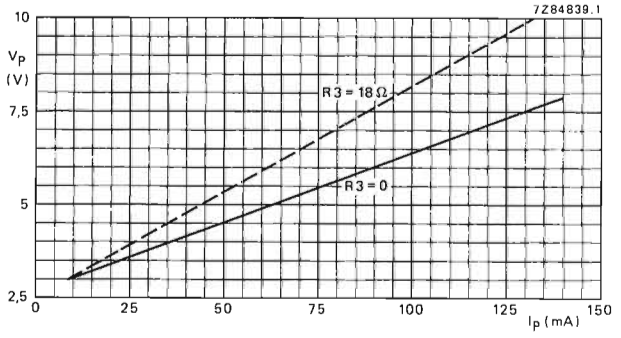
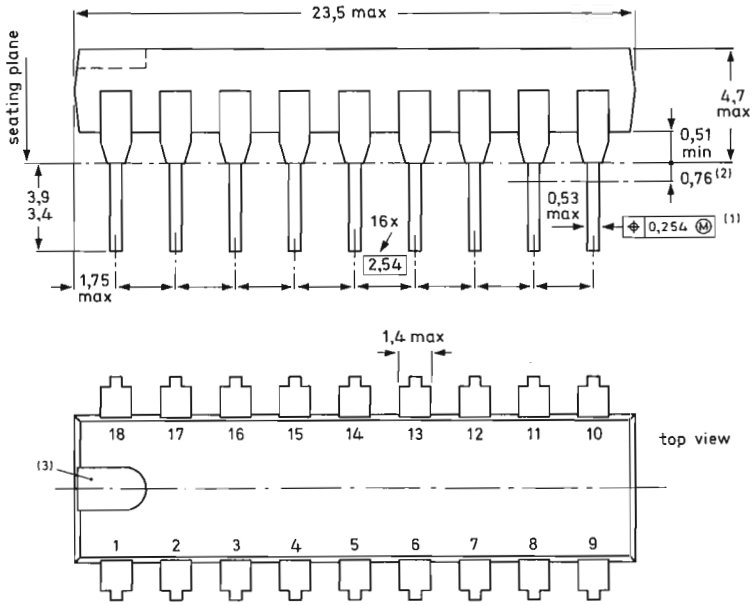
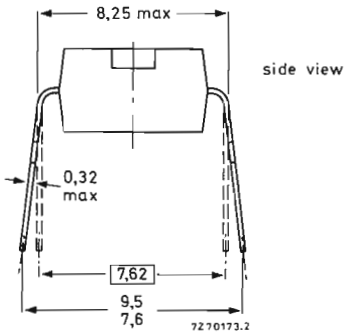


Fig. 10 D.C. characteristics.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)





⊕ Positional accuracy.

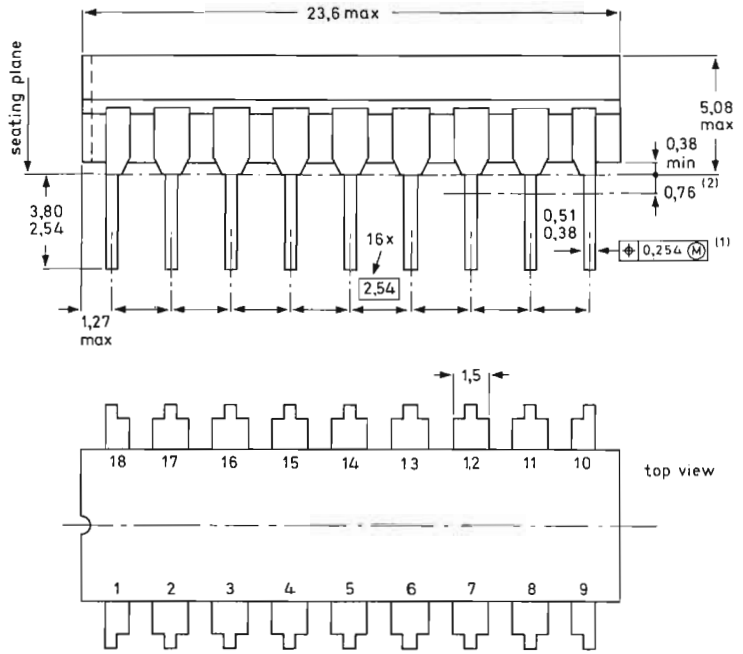
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

18-LEAD DUAL IN-LINE; CERAMIC (SOT-133)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

TELEPHONE TRANSMISSION CIRCUIT FOR HANDSFREE LOUDSPEAKING

GENERAL DESCRIPTION

The TEA1042 is a bipolar integrated circuit performing all speech and line interface functions in electronic telephone sets. It is especially designed for handsfree loudspeaking equipment.

Its features are:

- Supplied from telephone line current
- Voltage regulator with adjustable d.c. voltage drop and d.c. resistance
- High and low-impedance handset microphone inputs
- High-impedance base microphone input
- Handset/base selection input
- Muting input for pulse or DTMF dialling
- Gain setting facility on all amplifiers
- Line current dependent gain control facility with corrections for the exchange supply voltage and its feeding bridge resistance
- Supply output for additional circuits.

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{line}	typ.	4,2 V
Line current operating range	I_{line}		10 to 140 mA
Telephone line impedance	$\|Z_{line}\|$	nom.	600 Ω
Supply current	I_{CC}	typ.	1 mA
Voltage gain, transmitting amplifier			
MIC1 input	A_{vd}	typ.	44,1 dB
MIC2 input	A_{vd}	typ.	20 dB
MIC3 input	A_{vd}	typ.	20 dB
DTMF input	A_{vd}	typ.	25,6 dB
Voltage gain, receiving amplifier	A_{vd}	typ.	27 dB
Gain adjustment range			
transmitting amplifier	ΔA_{vd}	typ.	± 6 dB
receiving amplifier	ΔA_{vd}	typ.	± 8 dB
Range of gain control with line current, all amplifiers	ΔA_{vd}	typ.	6 dB
Exchange supply voltage range	V_{exch}		24 to 60 V
Exchange feeding bridge resistance	R_{exch}		400 or 800 Ω
Operating ambient temperature range	T_{amb}		−25 to + 70 °C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

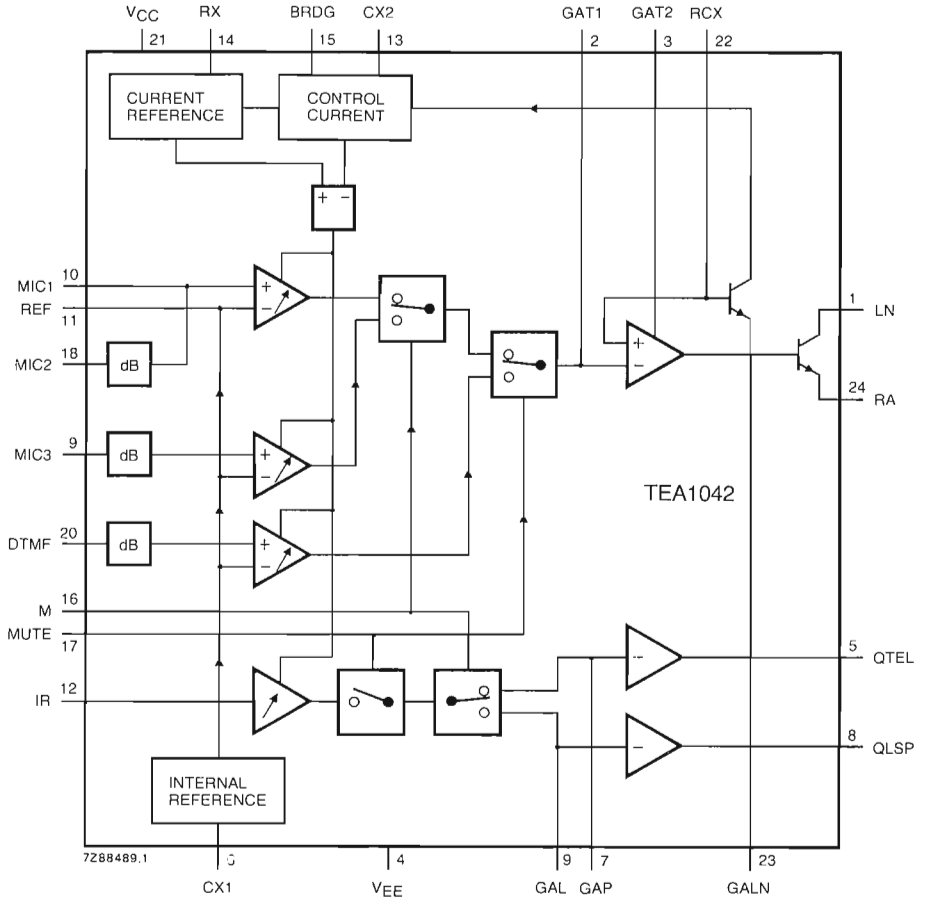


Fig. 1 Block diagram. The blocks marked dB are attenuators. The M and MUTE inputs operate analogue switches that activate or inhibit the inputs and outputs as required by their function.

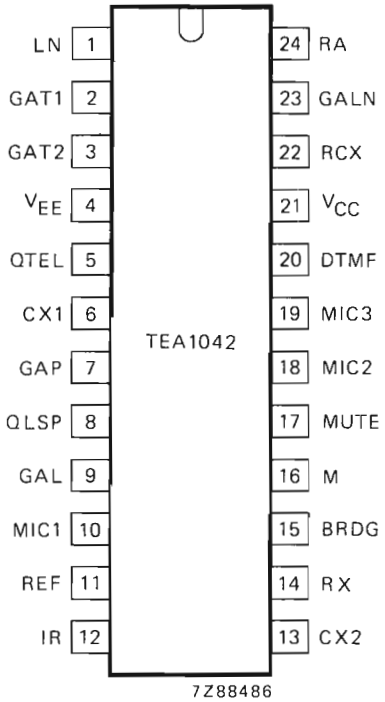


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAT1	gain adjustment; transmitting amplifier
3	GAT2	gain adjustment; transmitting amplifier
4	V_{EE}	negative line terminal
5	QTEL	handset telephone output
6	CX1	reference decoupling
7	GAP	gain adjustment; telephone amplifier
8	QLSP	loudspeaker preamplifier output
9	GAL	gain adjustment; loudspeaker preamplifier
10	MIC1	low-impedance handset microphone input
11	REF	reference voltage
12	IR	receiving amplifier input
13	CX2	external stabilizing capacitor
14	RX	external resistor
15	BRDG	selection input for gain control adaptation to feeding bridge impedance
16	M	mode (handset/base selection) input
17	MUTE	mute input
18	MIC2	high-impedance handset microphone input
19	MIC3	base microphone input
20	DTMF	dual-tone multi-frequency input
21	V_{CC}	positive supply
22	RCX	line voltage adjustment and voltage regulator decoupling
23	GALN	gain control with line current; all amplifiers
24	RA	d.c. resistance adjustment

FUNCTIONAL DESCRIPTION

The TEA1042 contains two receiving amplifiers, a transmitting amplifier, means to switch the inputs and the outputs, means to adjust the gain of all amplifiers individually, means to vary the gain with the line current and means to adjust the d.c. voltage drop and d.c. resistance. See the block diagram, Fig. 1.

Supply: LN, V_{CC}, V_{EE}, RA, CX1 and CX2 (pins 1, 21, 4, 24, 6 and 13)

The circuit is supplied from the line current, the arrangement is shown in Fig. 3. The circuit develops its own supply voltage at V_{CC} (pin 21). This supply voltage may also be used to supply an external circuit, e.g. a CMOS pulse or DTMF dialler or an electret microphone amplifier stage. The current available for this circuit depends on external components, see Fig. 4.

All line current has to flow through the circuit. If the line current exceeds the current required by the circuit itself via V_{CC} (pin 21), i.e. about 1 mA, plus the current required by the peripheral circuits connected to this pin, then the excess current is diverted via LN, the positive line terminal (pin 1), to RA (d.c. resistance adjustment; pin 24).

The minimum line voltage may be chosen by external resistor R5 and the variation with line current by external resistor R10. The circuit regulates the line voltage at T_{amb} = 25 °C to:

$$V_{line} = V_{LN} = \frac{R5 + R9}{R9} \times 0{,}62 + I_{LN} \times R10,$$

I_{LN} being the current diverted via LN.

A regulator decoupling capacitor has to be connected between RCX (pin 22) and V_{EE}, the negative line terminal (pin 4), a smoothing capacitor has to be connected between V_{CC} (pin 21) and V_{EE}, and a stabilizing capacitor between CX2 (pin 13) and V_{EE}. Further a decoupling capacitor has to be connected between CX1 (reference decoupling; pin 6) and V_{EE} (pin 4).

The dynamic impedance that the circuit presents to the line in the speech band is determined primarily by resistor R1 connected between LN (pin 1) and V_{CC} (pin 21).

Mode (handset/base selection) input M (pin 16)

The mode input permits selection of operation via the handset or via the base. A HIGH level on the M input or an open circuit selects handset operation, i.e. it activates the microphone inputs MIC1 and MIC2 and the handset telephone output QTEL. A LOW level on M selects the base microphone input MIC3 and the loudspeaker preamplifier output QLSP.

Microphone inputs MIC1, MIC2 and MIC3 (pins 10, 18 and 19)

Handset and base may be equipped with a sensitive microphone, e.g. an electret microphone with pre-amplifier. This has to be connected to the MIC2 or MIC3 input respectively. The available gain from these inputs is typ. 20 dB.

The handset may also be equipped with an insensitive low-impedance microphone, e.g. a dynamic or magnetic microphone. This has to be connected between MIC1 (pin 10) and (REF (pin 11). The available gain from this input is typ. 44,1 dB.

Dual-tone multi-frequency input DTMF and mute input MUTE (pins 20 and 17)

A HIGH level on the MUTE input inhibits all microphone inputs and the telephone and loudspeaker outputs QTEL and QLSP and enables the DTMF input, a LOW level does the reverse. Switching the MUTE input will not produce any clicks on the line or in the telephone or loudspeaker. The available gain from the DTMF input is typ. 25,6 dB.

Telephone output QTEL and loudspeaker preamplifier output QLSP (pins 5 and 8)

As described before, the M input determines which of the outputs QTEL and QLSP will be activated. The receiving amplifier input IR (pin 12) is the input for both outputs. For both outputs the available gain is typ. 27 dB. The output QTEL is intended for telephone capsules with an impedance of 150 Ω or more. The QLSP output is intended to drive a power amplifier. Its output impedance is less than 1 kΩ.

Gain adjustment: GAT1, GAT2, GAP and GAL (pins 2, 3, 7 and 9)

The gain of the transmitting amplifier may be adjusted by an external resistor R2 connected between GAT1 and GAT2 (pins 2 and 3; see Fig. 9). This adjustment influences the sensitivity of the inputs MIC1, MIC2, MIC3 and DTMF to the same amount. The gain is proportional to R2 and inversely proportional to R10 and R12.

The gain of the telephone amplifier may be adjusted by an external resistor R14 between GAP (pin 7) and CX1 (pin 6). The gain is proportional to R14 and inversely proportional to R12.

The gain of the loudspeaker preamplifier may be adjusted by an external resistor R13 between GAL (pin 9) and CX1 (pin 6). The gain is proportional to R13 and inversely proportional to R12.

Gain control with line current: GALN (pin 23)

The circuit offers a facility to automatically vary the gain of all its amplifiers with the line current. In this way the circuit compensates for differences in line attenuation. The variation is accomplished by connecting an external resistor R11 between GALN (pin 23) and V_{EE} (pin 4). The value of this resistor should be chosen in accordance with the supply voltage of the exchange (see Figs 5 and 6).

If no gain variation with line current is required the GALN connection may be left open. All amplifiers have their maximum gain then.

Selection input for gain control adaptation to feeding bridge impedance: BRDG (pin 15)

A LOW level at the BRDG input optimizes the gain control characteristics of the circuit for a 400 Ω feeding bridge in the exchange, a HIGH level for 800 Ω.

Side tone suppression

In the circuit diagram shown in Fig. 9 side tone suppression is obtained with components C2, R3, R4, R7 and R8. Their component values have to be chosen to suit the cable type used. This network attenuates the signal from the telephone line to the IR input of the receiving amplifier. This attenuation may be adjusted by choosing the value of R7 without affecting the side tone suppression.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current			
d.c.	I_{line}	max.	140 mA
non-repetitive ($t < 100$ h)	I_{line}	max.	250 mA
Storage temperature range	T_{stg}	−40 to +125	°C
Operating ambient temperature range	T_{amb}	−25 to +70	°C
Junction temperature	T_j	max.	150 °C

CHARACTERISTICS

I_{line} = 10 to 140 mA; f = 1000 Hz; T_{amb} = 25 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 21)					
Line voltage					
I_{line} = 15 mA	V_{line}	4	4,2	4,4	V
I_{line} = 50 mA	V_{line}	–	–	5,8	V
I_{line} = 100 mA	V_{line}	–	–	7,3	V
Variation with temperature	$-\Delta V_{line}/\Delta T$	8	10	12	mV/K
Line current operating rage	I_{line}	10	–	140	mA
Supply current at V_{CC} = 2 V	I_{CC}	–	–	1	mA
Mode (handset/base selection) input M (pin 16)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{16}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Low-impedance handset microphone input MIC1 and reference voltage pin REF (pins 10 and 11)					
Input impedance	$\lvert Z_{10\text{-}11}\rvert$	–	3	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	43,1	44,1	45,1	dB
High-impedance handset microphone input MIC2 (pin 18)					
Input impedance	$\lvert Z_{18\text{-}4}\rvert$	40	48	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	19	20	21	dB
Base microphone input MIC3 (pin 19)					
Input impedance	$\lvert Z_{19\text{-}4}\rvert$	40	48	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	19	20	21	dB
DTMF input (pin 20)					
Input impedance	$\lvert Z_{20\text{-}4}\rvert$	10	15	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	24,6	25,6	26,6	dB
Gain adjustment pins; transmitting amplifier: GAT1 and GAT2 (pins 2 and 3)					
Gain adjustment range	ΔA_{vd}	–	± 6	–	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA; R_{line} = 600 Ω; d = 2%	$v_{LN(rms)}$	1,4	–	–	V
Psophometrically weighted* noise output voltage at I_{line} = 15 mA; R_{line} = 600 Ω	$v_{LN(rms)}$	–	245	–	μV
MUTE input (pin 17)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{17}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Receiving amplifier input IR (pin 12)					
Input impedance	$\|Z_{12-4}\|$	–	10	–	kΩ
Telephone output QTEL (pin 5)					
Voltage gain at I_{line} = 15 mA; R_{load} = 150 Ω; R13 = 15 kΩ; see Fig. 8	A_{vd}	26	27	28	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB
Maximum output voltage at I_{line} = 15 mA; R_{load} = 150 Ω; d = 2%	$v_{O(rms)}$	350	–	–	mV
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Gain adjustment pin; telephone amplifier: GAP (pin 7)					
Gain adjustment range	ΔA_{vd}	–	± 8	–	dB
Loudspeaker preamplifier output QLSP (pin 8)					
Voltage gain at I_{line} = 15 mA; R_{load} = 10 kΩ; R14 = 15 kΩ; see Fig. 8	A_{vd}	–	27	–	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature	ΔA_{vd}	–	± 0,5	–	dB
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Output impedance	$\|Z_{8-4}\|$	–	–	1	kΩ
Gain adjustment pin; loudspeaker preamplifier: GAL (pin 9)					
Gain adjustment range	ΔA_{vd}	–	± 8	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Selection input for gain control adaptation to feeding bridge impedance BRDG (pin 15)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{15}$	–	8	20	μA
Gain control with line current pin GALN (pin 23)					
Gain control range	ΔA_{vd}	–	6	–	dB
Highest line current for maximum gain, R11 = 105 kΩ;					
BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	22,5	25	27,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	31,5	35	38,5	mA
Lowest line current for minimum gain, R11 = 105 kΩ;					
BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	49,5	55	60,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	81	90	99	mA

* P53 curve.

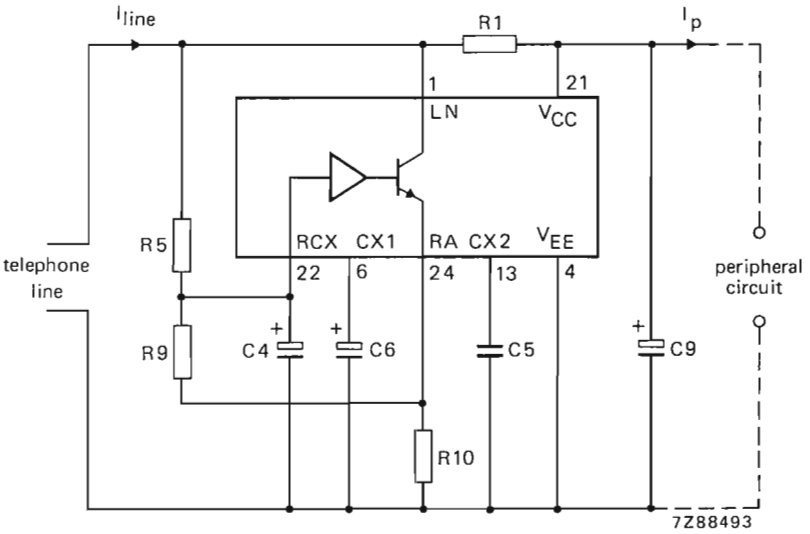


Fig. 3 Supply arrangement.

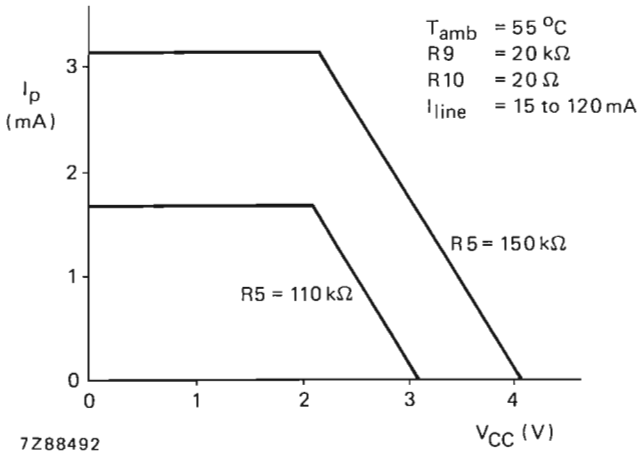


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuits.

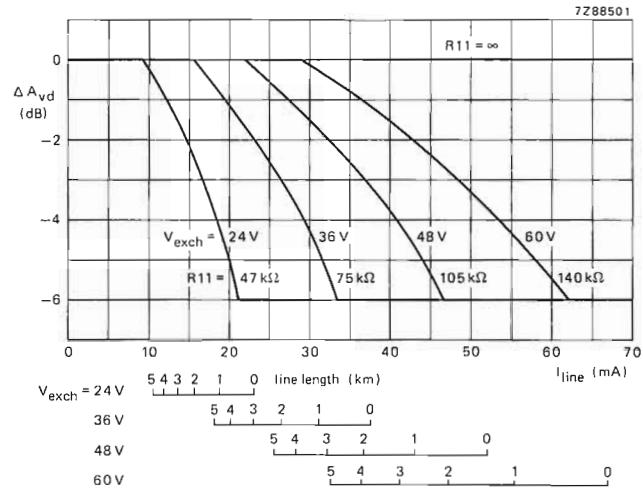


Fig. 5 Gain variation with line current, with R11 as a parameter, and with the BRDG input HIGH, i.e. the circuit optimized for 800 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

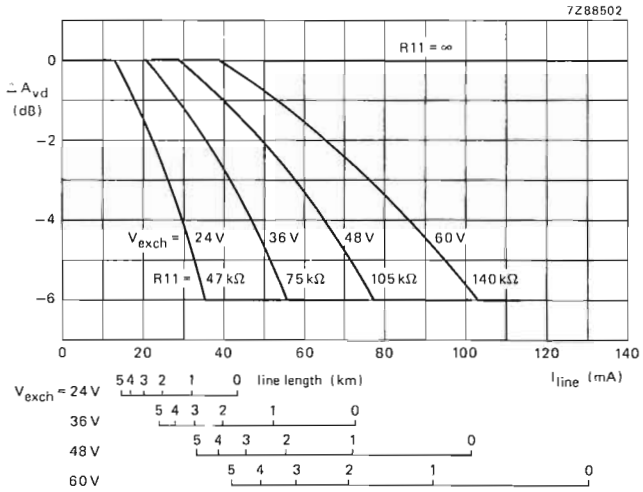


Fig. 6 Gain variation with line current, with R11 as a parameter, and with the BRDG input LOW, i.e. the circuit optimized for 400 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

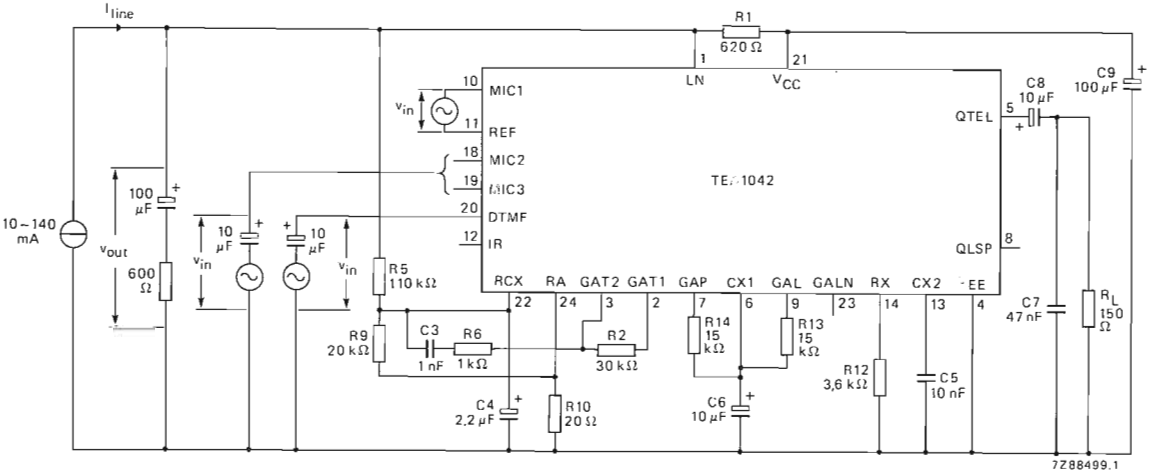


Fig. 7 Test circuit for defining voltage gain of MIC1, MIC2, MIC3 and DTMF inputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the MIC1 or MIC2 input the M input should be HIGH and the MUTE input LOW, for measuring the MIC3 input M and MUTE should both be LOW and for measuring the DTMF input M and MUTE should be HIGH. Inputs not under test should be open.

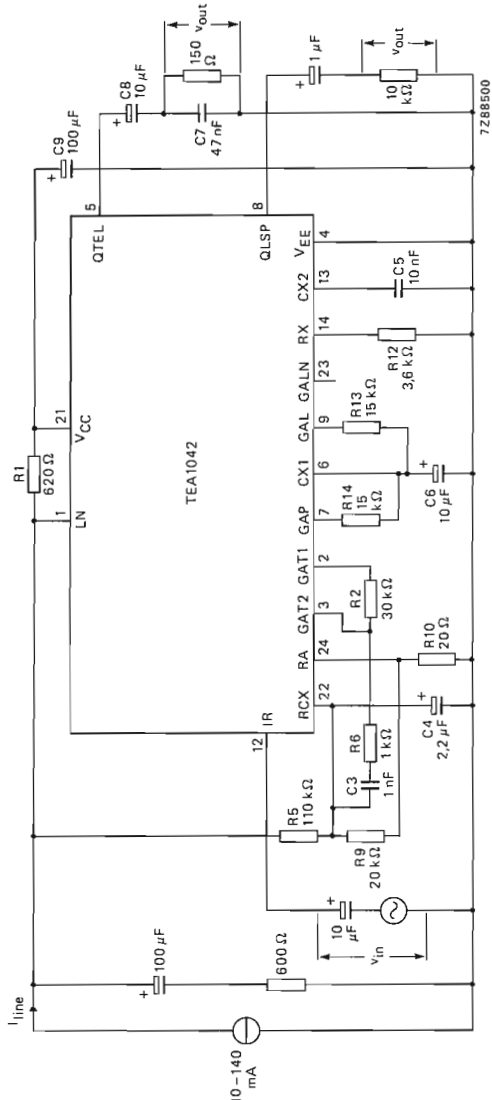


Fig. 8 Test circuit for defining voltage gain of QTEL and QLSP outputs. Gain is defined as: $A_{vd} = 20 \log |V_{out}/V_{in}|$. For measuring the QTEL output the M input should be HIGH and the MUTE input LOW, for measuring the QLSP output M and MUTE should both be LOW.

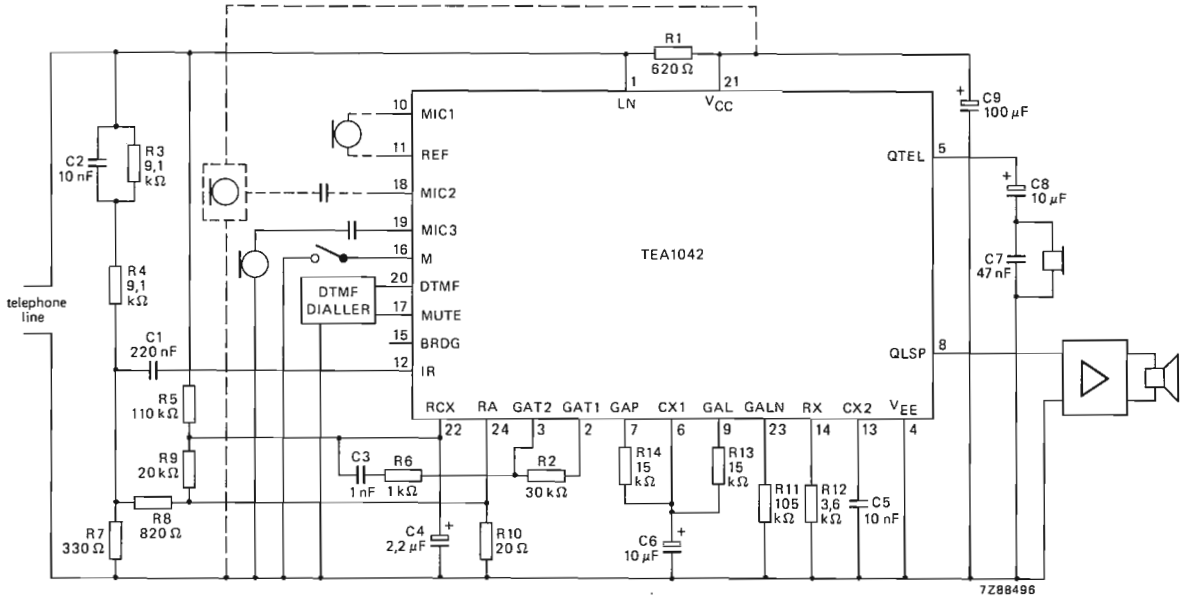
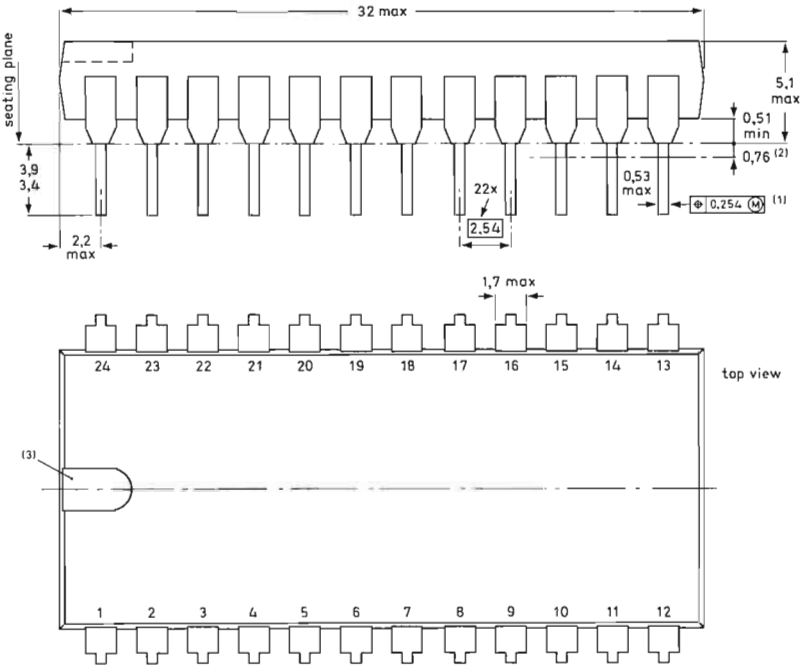
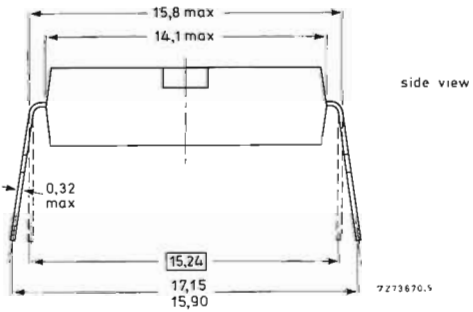


Fig. 9 Typical application of the TEA1042 in an electronic handsfree telephone set. The connections to the MIC1 and MIC2 inputs are alternatives. The connection to the BRDG input is not shown, see the Functional Description. The diagram does not show voice switches and associated control circuits required in a practical circuit for stable loudspeaking operation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See next page.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

TELEPHONE TRANSMISSION CIRCUIT

GENERAL DESCRIPTION

The TEA1053 and TEA1054 are bipolar integrated circuits performing all speech and line interface functions in electronic telephone sets.

Their features are:

- Supplied from telephone line current
- Voltage regulator with adjustable d.c. voltage drop and d.c. resistance
- Low-impedance microphone input
- Muting input for pulse or DTMF dialling
- Gain setting facility on all amplifiers
- Line current dependent gain control facility with corrections for the exchange supply voltage
- Supply output for additional circuits

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{line}	typ. 4,2	V
Line current operating range	I_{line}	10 to 140	mA
Telephone line impedance	$\|Z_{line}\|$	nom. 600	Ω
Supply current	I_{CC}	typ. 1	mA
Voltage gain, transmitting amplifier			
MIC input	A_{vd}	typ. 44,1	dB
DTMF input	A_{vd}	typ. 25,6	dB
Voltage gain, receiving amplifier	A_{vd}	typ. 27	dB
Gain adjustment range			
transmitting amplifier	ΔA_{vd}	typ. ± 6	dB
receiving amplifier	ΔA_{vd}	typ. ± 8	dB
Range of gain control with line current, all amplifiers	ΔA_{vd}	typ. 6	dB
Exchange supply voltage range	V_{exch}	24 to 60	V
Exchange feeding bridge resistance			
TEA1053	R_{exch}	800	Ω
TEA1054	R_{exch}	400	Ω
Operating ambient temperature range	T_{amb}	−25 to +70	°C

PACKAGE OUTLINE

TEA1053; TEA1054: 18-lead DIL; plastic (SOT-102A).

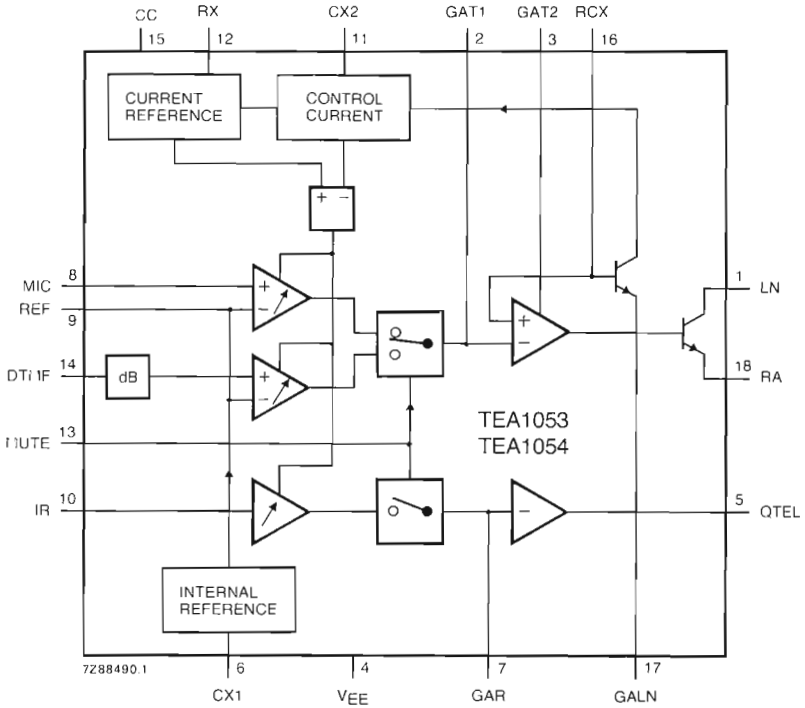


Fig. 1 Block diagram. The blocks marked dB are attenuators. The MUTE input operates analogue switches that activate or inhibit the inputs and outputs as required by the function of the MUTE input.

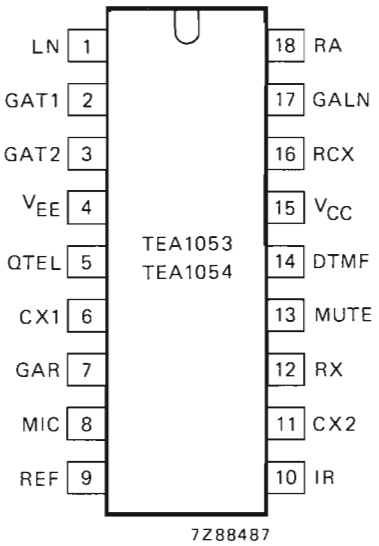


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line connection
2	GAT1	gain adjustment connection, transmitting amplifier
3	GAT2	gain adjustment connection, transmitting amplifier
4	V_{EE}	negative line connection
5	QTEL	telephone output
6	CX1	reference decoupling connection
7	GAR	gain adjustment connection, receiving amplifier
8	MIC	microphone input
9	REF	reference voltage connection
10	IR	receiving amplifier input
11	CX2	external stabilizing capacitor connection
12	RX	external resistor connection
13	MUTE	mute input
14	DTMF	dual-tone multi-frequency input
15	V_{CC}	positive supply connection
16	RCX	line voltage adjustment and voltage regulator decoupling connection
17	GALN	gain control with line current connection, all amplifiers
18	RA	d.c. resistance adjustment connection

DEVELOPMENT SAMPLE DATA

FUNCTIONAL DESCRIPTION

The TEA1053 and TEA1054 contain a receiving amplifier, a transmitting amplifier, means to switch the inputs, means to adjust the gain of the amplifiers individually, means to vary the gain with the line current and means to adjust the d.c. voltage drop and d.c. resistance. See the block diagram, Fig. 1.

Supply: LN, V_{CC}, V_{EE}, RA, CX1 and CX2 (pins 1, 15, 4, 18, 6 and 11)

The circuit is supplied from the line current, the arrangement is shown in Fig. 3. The circuit develops its own supply voltage at V_{CC}, the positive supply connection, pin 15. This supply voltage may also be used to supply an external circuit, e.g. a CMOS pulse or DTMF dialler. The current available for this circuit depends on external components, see Fig. 4.

All line current has to flow through the circuit. If the line current exceeds the current required by the circuit itself via V_{CC}, pin 15, i.e. about 1 mA, plus the current required by the peripheral circuits connected to this pin, then the excess current is diverted via LN, the positive line connection, pin 1, to RA, the d.c. resistance adjustment connection, pin 18.

The minimum line voltage may be chosen by external resistor R5 and the variation with line current by external resistor R10. The circuit regulates the line current at 25 °C to:

$$V_{line} = V_{LN} = \frac{R5 + R9}{R9} \times 0{,}62 + I_{LN} \times R10,$$

I_{LN} being the current diverted via LN, the positive line connection.

A regulator decoupling capacitor has to be connected between RCX, pin 16, and V_{EE}, the negative line connection, pin 4, a smoothing capacitor has to be connected between V_{CC}, pin 15, and V_{EE}, and a stabilizing capacitor between CX2, pin 11 and V_{EE}, pin 4. Further a decoupling capacitor has to be connected between CX1, the reference decoupling connection, pin 6, and V_{EE}, pin 4.

The dynamic impedance that the circuit presents to the line in the speech band is determined primarily by resistor R1 connected between LN, pin 1, and V_{CC}, pin 15.

Microphone input MIC (pin 8)

The MIC input has a low input impedance, especially suited for a dynamic or magnetic microphone. This has to be connected between MIC, pin 8, and REF, pin 9. The available gain is typ. 44,1 dB.

Dual-tone multi-frequency input DTMF and mute input MUTE (pins 14 and 13)

A HIGH level on the MUTE input inhibits the microphone input MIC and the telephone outputs QTEL and enables the DTMF input, a LOW level does the reverse. Switching the MUTE input will not produce any clicks on the line or in the telephone. The available gain from the DTMF input is typ. 25,6 dB.

Receiving amplifier input IR and telephone output QTEL (pins 10 and 5)

The available gain from input IR to output QTEL is typ. 27 dB. The output QTEL is intended for telephone capsules with an impedance of 150 Ω or more.

Gain adjustment connections GAT1, GAT2, and GAR (pins 2, 3 and 7)

The gain of the transmitting amplifier may be adjusted by an external resistor R2 connected between GAT1 and GAT2, pins 2 and 3 (see Fig. 9). This adjustment influences the sensitivity of the inputs MIC and DTMF to the same amount. The gain is proportional to R2 and inversely proportional to R10 and R12.

The gain of the receiving amplifier may be adjusted by an external resistor R14 between GAR, pin 7, and CX1, pin 6. The gain is proportional to R14 and inversely proportional to R12.

Gain control with line current, GALN connection (pin 17)

The circuit offers a facility to automatically vary the gain of all its amplifiers with the line current. In this way the circuit compensates for differences in line attenuation. The variation is accomplished by connecting an external resistor R11 between GALN, pin 17, and V_{EE}, pin 4. The value of this resistor should be chosen in accordance with the supply voltage of the exchange (see Figs 5 and 6).

If no gain variation with line current is required the GALN connection may be left open. All amplifiers have their maximum gain then.

Side tone suppression

In the circuit diagram shown in Fig. 9 side tone suppression is obtained with components C2, R3, R4, R7 and R8. Their component values have to be chosen to suit the cable type used. This network attenuates the signal from the telephone line to the IR input of the receiving amplifier. This attenuation may be adjusted by choosing the value of R7 without affecting the side tone suppression.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply current				
d.c.	I_{line}	max.	140	mA
surge, $t < 100$ h	I_{line}	max.	250	mA
Storage temperature range	T_{stg}	−40 to	+125	°C
Operating temperature range	T_{amb}	−25 to	+70	°C
Junction temperature	T_j	max.	150	°C

CHARACTERISTICS

I_{line} = 10 to 140 mA; f = 1 kHz; T_{amb} = 25 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit
Supply, LN and V_{CC} (pins 1 and 15)					
Line voltage					
I_{line} = 15 mA	V_{line}	4	4,2	4,4	V
I_{line} = 50 mA	V_{line}	–	–	5,8	V
I_{line} = 100 mA	V_{line}	–	–	7,3	V
Variation with temperature	$-\Delta V_{line}/\Delta T$	8	10	12	mV/K
Line current operating range	I_{line}	10	–	140	mA
Supply current at V_{CC} = 2 V	I_{CC}	–	–	1	mA
Microphone input MIC and reference voltage connection REF (pins 8 and 9)					
Input impedance	$\lvert Z_{8\text{-}9}\rvert$	–	3	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	43,1	44,1	45,1	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = –5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB
DTMF input (pin 14)					
Input impedance	$\lvert Z_{14\text{-}4}\rvert$	10	15	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	24,6	25,6	26,6	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = –5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB
Gain adjustment connections, transmitting amplifier, GAT1 and GAT2 (pins 2 and 3)					
Gain adjustment range	ΔA_{vd}	–	± 6	–	dB
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA; R_{line} = 600 Ω d = 2%	$v_{LN(rms)}$	1,4	–	–	V
Psophometrically weighted * noise output voltage at I_{line} = 15 mA; R_{line} = 600 Ω	$v_{LN(rms)}$	–	245	–	μV

	symbol	min.	typ.	max.	unit
MUTE input (pin 13)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{13}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Receiving amplifier input IR (pin 10)					
Input impedance	$\lvert Z_{10\text{-}4}\rvert$	–	10	–	kΩ
Telephone output QTEL (pin 5)					
Voltage gain at I_{line} = 15 mA; R_{load} = 150 Ω; R14 = 7,5 kΩ; see Fig. 8	A_{vd}	26	27	28	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	± 0,5	–	dB
Maximum output voltage at I_{line} = 15 mA; R_{load} = 150 Ω; d = 2%	$v_{O(rms)}$	350	–	–	mV
Psophometrically weighted * noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Gain adjustment connection, receiving amplifier, GAR (pin 7)					
Gain adjustment range	ΔA_{vd}	–	± 8	–	dB
Gain control with line current connection GALN (pin 17)					
Gain control range	ΔA_{vd}	–	6	–	dB
Highest line current for maximum gain, R11 = 105 kΩ; TEA1053	I_{line}	22,5	25	27,5	mA
TEA1054	I_{line}	31,5	35,5	38,5	mA
Lowest line current for minimum gain, R11 = 105 kΩ; TEA1053	I_{line}	49,5	55	60,5	mA
TEA1054	I_{line}	81	90	99	mA

DEVELOPMENT SAMPLE DATA

* P53 curve.

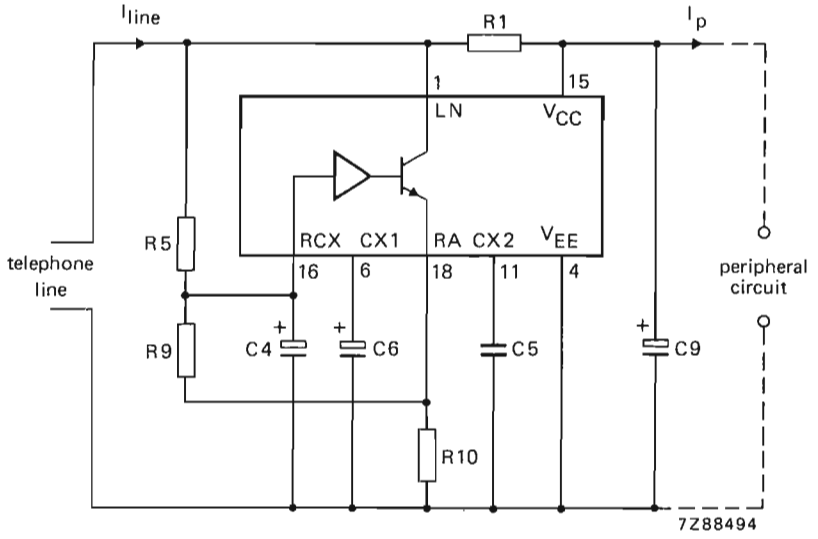


Fig. 3 Supply arrangement.

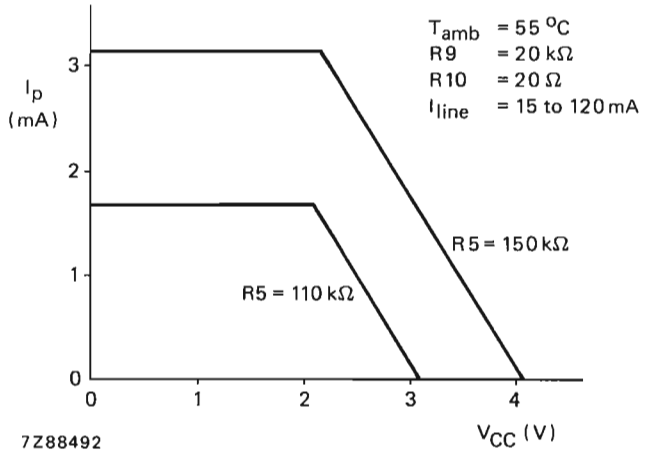


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuits.

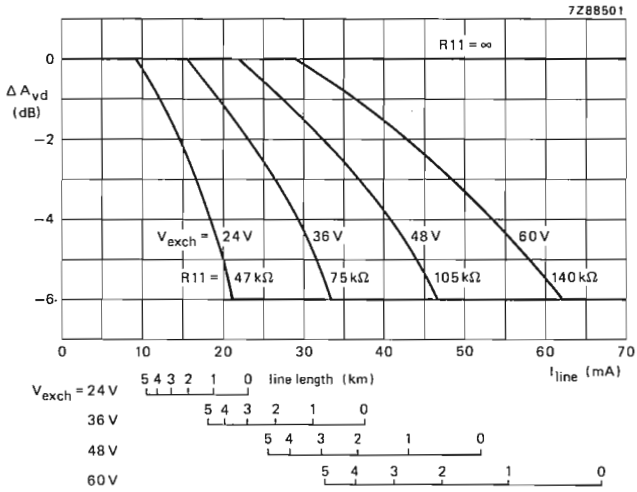


Fig. 5 Gain variation with line current for the TEA1053, with R11 as a parameter. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

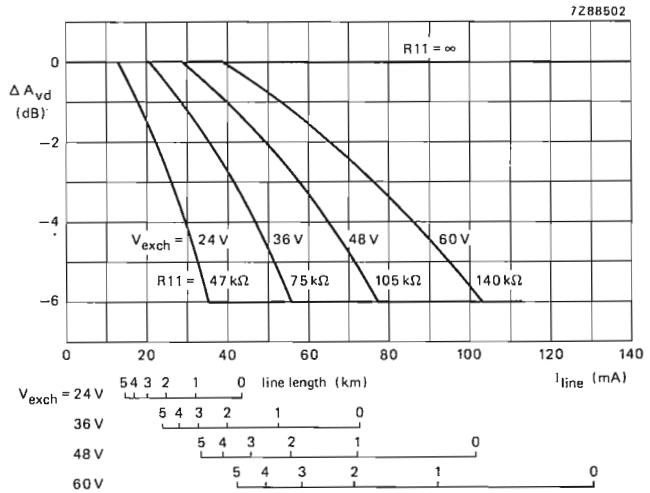


Fig. 6 Gain variation with line current for the TEA1054, with R11 as a parameter. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

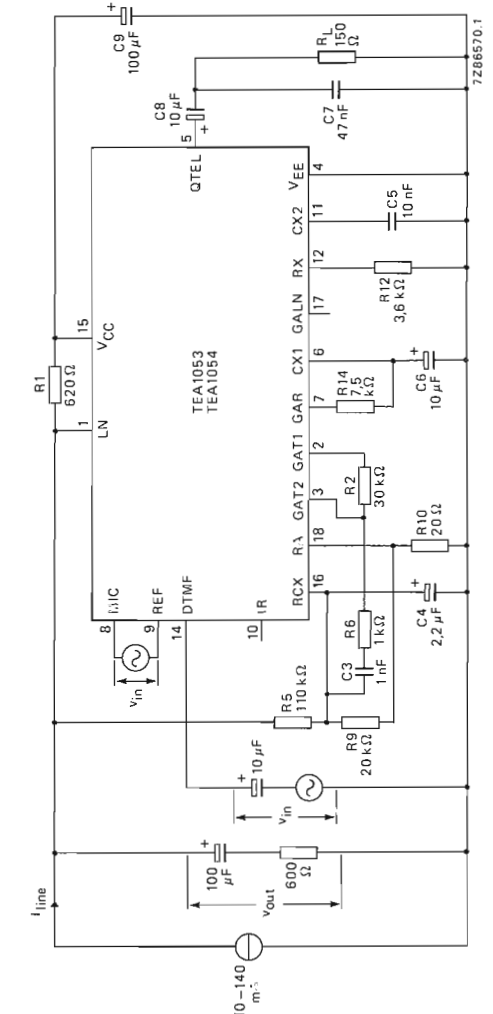


Fig. 7 Test circuit for defining voltage gain of MIC and DTMF inputs. Gain is defined as: $A_{vd} = 20 \log |V_{out}/V_{in}|$. For measuring the MIC input the MUTE input should be LOW and for measuring the DTMF input MUTE should be HIGH. The input not under test should be open.

PHILIPS

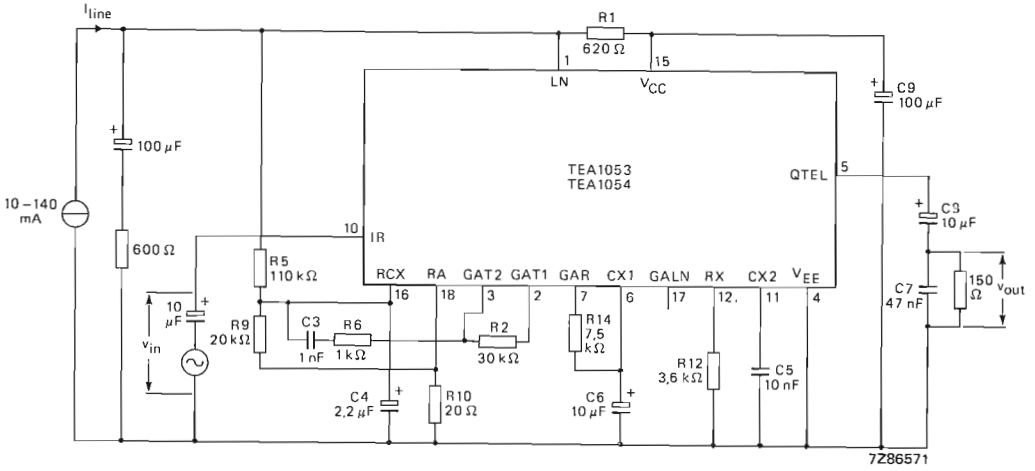


Fig. 8 Test circuit for defining voltage gain of the receiving amplifier. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. The MUTE input should be LOW.

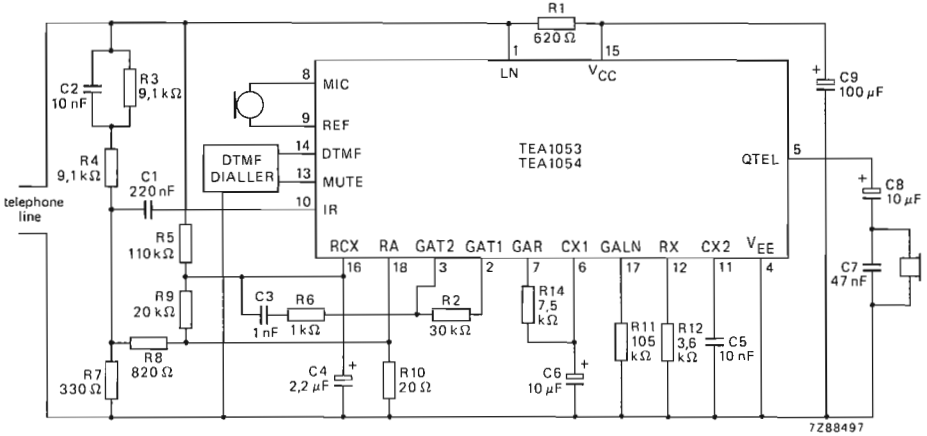
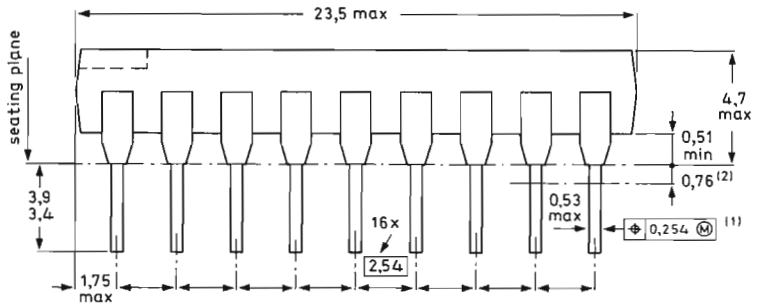
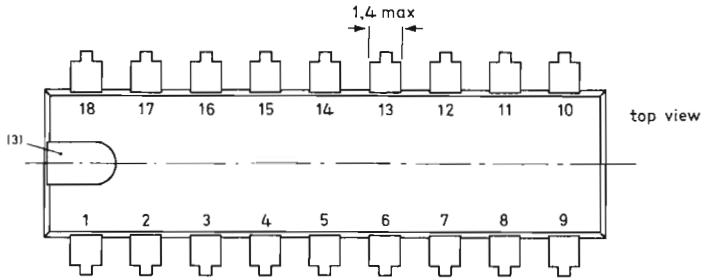


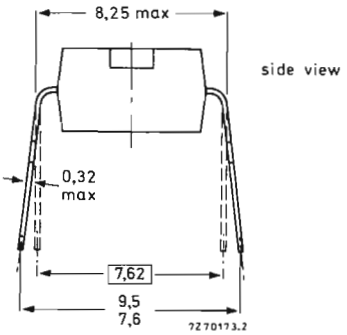
Fig. 9 Typical application of the TEA1053 or TEA1054 in an electronic telephone set.

APPLICATION INFORMATION SUPPLIED ON REQUEST.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)







⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See next page.

DEVELOPMENT SAMPLE DATA

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

TELEPHONE TRANSMISSION CIRCUIT

GENERAL DESCRIPTION

The TEA1055 is a bipolar integrated circuit performing the speech and line interface functions in electronic telephone sets.

Its features are:

- Supplied from telephone line current
- Voltage regulator with adjustable d.c. voltage drop and d.c. resistance
- High-impedance microphone input
- Muting input for pulse or DTMF dialling
- Gain setting facility on all amplifiers
- Line current dependent gain control facility with corrections for the exchange supply voltage and its feeding bridge resistance
- Supply output for additional circuits

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{line}	typ. 4,2	V
Line current operating range	I_{line}	10 to 140	mA
Telephone line impedance	$\|Z_{line}\|$	nom. 600	Ω
Supply current	I_{CC}	typ. 1	mA
Voltage gain, transmitting amplifier			
MIC input	A_{vd}	typ. 20	dB
DTMF input	A_{vd}	typ. 25,6	dB
Voltage gain, receiving amplifier	A_{vd}	typ. 27	dB
Gain adjustment range			
transmitting amplifier	ΔA_{vd}	typ. ± 6	dB
receiving amplifier	ΔA_{vd}	typ. ± 8	dB
Range of gain control with line current, all amplifiers	ΔA_{vd}	typ. 6	dB
Exchange supply voltage range	V_{exch}	24 to 60	V
Exchange feeding bridge resistance	R_{exch}	400 or 800	Ω
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINE

TEA1055: 18-lead DIL; plastic (SOT-102A).

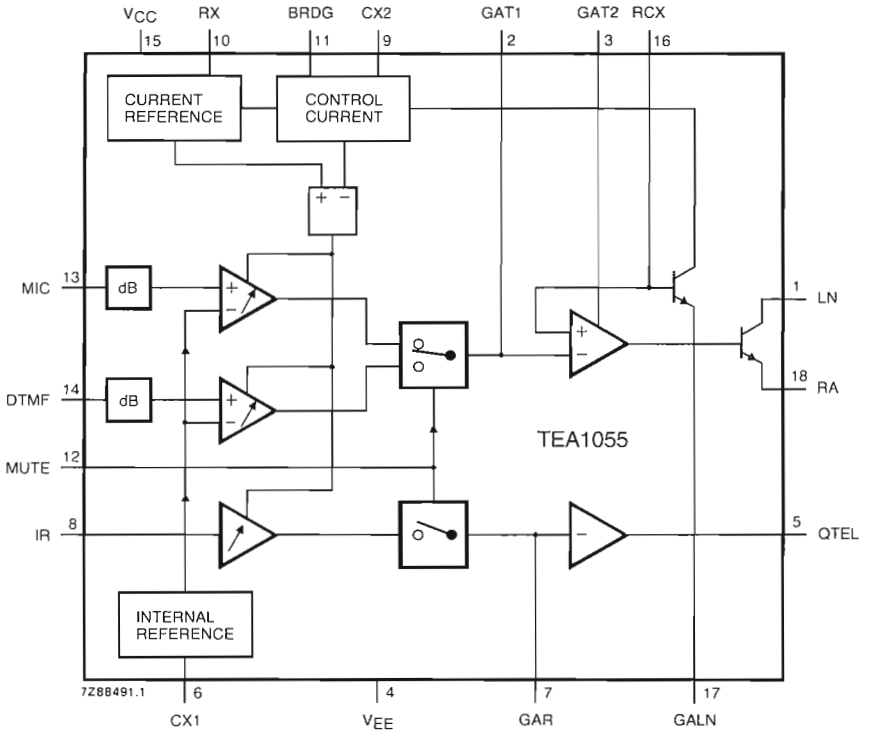


Fig. 1 Block diagram. The blocks marked dB are attenuators. The MUTE input operates analogue switches that activate or inhibit the inputs and outputs as required by the function of the MUTE input.

PINNING

1	LN	positive line connection
2	GAT1	gain adjustment connection, transmitting amplifier
3	GAT2	gain adjustment connection, transmitting amplifier
4	V_{EE}	negative line connection
5	QTEL	telephone output
6	CX1	reference decoupling connection
7	GAR	gain adjustment connection, receiving amplifier
8	IR	receiving amplifier input
9	CX2	external stabilizing capacitor connection
10	RX	external resistor connection
11	BRDG	selection input for gain control adaption to feeding bridge impedance
12	MUTE	mute input
13	MIC	microphone input
14	DTMF	dual-tone multi-frequency input
15	V_{CC}	positive supply connection
16	RCX	line voltage adjustment and decoupling connection
17	GALN	gain control with line current connection, all amplifiers
18	RA	d.c. resistance adjustment connection

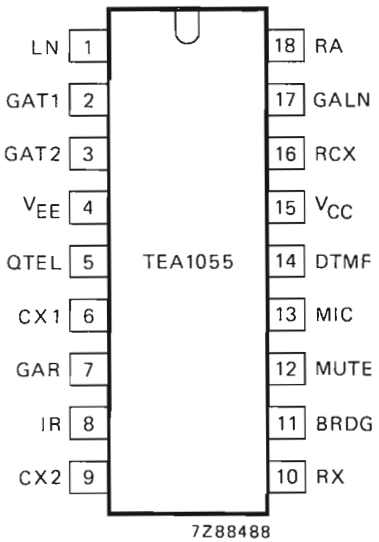


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TEA1055 contains a receiving amplifier, a transmitting amplifier, means to switch the inputs, means to adjust the gain of the amplifiers individually, means to vary the gain with the line current and means to adjust the d.c. voltage drop and d.c. resistance. See the block diagram, Fig. 1.

Supply: LN, V_{CC}, V_{EE}, RA, CX1 and CX2 (pins 1, 15, 4, 18, 6 and 9)

The circuit is supplied from the line current, the arrangement is shown in Fig. 3. The circuit develops its own supply voltage at V_{CC}, the positive supply connection, pin 15. This supply voltage may also be used to supply an external circuit, e.g. an electret microphone amplifier stage or a CMOS pulse or DTMF dialler. The current available for this circuit depends on external components, see Fig. 4.

All line current has to flow through the circuit. If the line current exceeds the current required by the circuit itself via V_{CC}, pin 15, i.e. about 1 mA, plus the current required by the peripheral circuits connected to this pin, then the excess current is diverted via LN, the positive line connection, pin 1, to RA, the d.c. resistance adjustment connection, pin 18.

The minimum line voltage may be chosen by external resistor R5 and the variation with line current by external resistor R10. The circuit regulates the line voltage at $T_{amb} = 25\ ^{o}C$ to:

$$V_{line} = V_{LN} = \frac{R5 + R9}{R9} \cdot 0{,}62 + I_{LN} \cdot R10,$$

I_{LN} being the current diverted via LN, the positive line connection.

A regulator decoupling capacitor has to be connected between RCX, pin 16, and V_{EE}, the negative line connection, pin 4, a smoothing capacitor has to be connected between V_{CC}, pin 15, and V_{EE}, and a stabilizing capacitor between CX2, pin 9 and V_{EE}, pin 4. Further a decoupling capacitor has to be connected between CX1, the reference decoupling connection, pin 6, and V_{EE}, pin 4.

The dynamic impedance that the circuit presents to the line in the speech band is determined primarily by resistor R1 connected between LN, pin 1, and V_{CC}, pin 15.

Microphone input MIC (pin 13)

The circuit has a high-impedance microphone input, especially suited for a sensitive microphone, e.g. an electret microphone with preamplifier. The available gain is typ. 20 dB.

Dual-tone multi-frequency input DTMF and mute input MUTE (pins 14 and 12)

A HIGH level on the MUTE input inhibits the microphone input and the telephone output QTEL and enables the DTMF input, a LOW level does the reverse. Switching the MUTE input will not produce any clicks on the line or in the telephone. The available gain from the DTMF input is typ. 25,6 dB.

Receiving amplifier input IR and telephone output QTEL (pins 8 and 5)

The output QTEL is intended for telephone capsules with an impedance of 150 Ω or more. The available gain is typ. 27 dB.

Gain adjustment connections GAT1, GAT2 and GAR (pins 2, 3 and 7)

The gain of the transmitting amplifier may be adjusted by an external resistor R2 connected between GAT1 and GAT2, pins 2 and 3 (see Fig. 9). This adjustment influences the sensitivity of the inputs MIC and DTMF to the same amount. The gain is proportional to R2 and inversely proportional to R10 and R12.

The gain of the receiving amplifier may be adjusted by an external resistor R14 between GAR, pin 7, and CX1, pin 6. The gain is proportional to R14 and inversely proportional to R12.

Gain control with line current, GALN connection (pin 17)

The circuit offers a facility to automatically vary the gain of all its amplifiers with the line current. In this way the circuit compensates for differences in line attenuation. The variation is accomplished by connecting an external resistor R11 between GALN, pin 17, and V_{EE}, pin 4. The value of this resistor should be chosen in accordance with the supply voltage of the exchange and its feeding bridge resistance (see Figs 5 and 6).

If no gain variation with line current is required the GALN connection may be left open. All amplifiers have their maximum gain then.

Selection input for gain control adaption to feeding bridge impedance, BRDG (pin 11)

A LOW level at the BRDG input optimized the gain control characteristics of the circuit for a 400 Ω feeding bridge in the exchange, a HIGH level for 800 Ω.

Side tone suppression

In the circuit diagram shown in Fig. 9 side tone suppression is obtained with components C2, R3, R4, R7 and R8. Their component values have to be chosen to suit the cable type used. This network attenuates the signal from the telephone line to the IR input of the receiving amplifier. This attenuation may be adjusted by choosing the value of R7 without affecting the side tone suppression.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current			
d.c.	I_{line}	max.	140 mA
surge, $t < 100$ h	I_{line}	max.	250 mA
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating temperature range	T_{amb}	−25 to + 70	°C
Junction temperature	T_j	max.	150 °C

CHARACTERISTICS

I_{line} = 10 to 140 mA; f = 1 kHz; T_{amb} = 25 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit
Supply, LN and V_{CC} (pins 1 and 15)					
Line voltage					
I_{line} = 15 mA	V_{line}	4	4,2	4,4	V
I_{line} = 50 mA	V_{line}	–	–	5,8	V
I_{line} = 100 mA	V_{line}	–	–	7,3	V
Variation with temperature	$-\Delta V_{line}/\Delta T$	8	10	12	mV/K
Line current operating range	I_{line}	10	–	140	mA
Supply current at V_{CC} = 2 V	I_{CC}	–	–	1	mA
Microphone input MIC (pin 13)					
Input impedance	$\|Z_{13\text{-}4}\|$	40	48	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	19	20	21	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to + 45 °C	ΔA_{vd}	–	± 0,5	–	dB
DTMF input (pin 14)					
Input impedance	$\|Z_{14\text{-}4}\|$	10	15	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	24,6	25,6	26,6	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to + 45 °C	ΔA_{vd}	–	± 0,5	–	dB
Gain adjustment connections, transmitting amplifier, GAT1 and GAT2 (pins 2 and 3)					
Gain adjustment range	ΔA_{vd}	–	± 6	–	dB
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA; R_{line} = 600 Ω d = 2%	$V_{LN(rms)}$	1,4	–	–	V
Psophometrically weighted* noise output voltage at I_{line} = 15 mA; R_{line} = 600 Ω	$V_{LN(rms)}$	–	245	–	μV
MUTE input (pin 12)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{12}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB

	symbol	min.	typ.	max.	unit
Receiving amplifier input IR (pin 8)					
Input impedance	$\lvert Z_{8\text{-}4}\rvert$	–	10	–	kΩ
Telephone output QTEL (pin 5)					
Voltage gain at I_{line} = 15 mA; R_{load} = 150 Ω; R14 = 7,5 kΩ; see Fig. 8	A_{vd}	26	27	28	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	± 0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to + 45 °C	ΔA_{vd}	–	± 0,5	–	dB
Maximum output voltage at I_{line} = 15 mA; R1 = 150 Ω; d = 2%	$V_{O(rms)}$	350	–	–	mV
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$V_{O(rms)}$	–	40	–	μV
Gain adjustment connection, receiving amplifier, GAR (pin 7)					
Gain adjustment range	ΔA_{vd}	–	± 8	–	dB
Selection input for gain control adaption to feeding bridge impedance, BRDG (pin 11)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{11}$	–	8	20	μA
Gain control with line current connection GALN (pin 17)					
Gain control range	ΔA_{vd}	–	6	–	dB
Highest line current for maximum gain, R11 = 105 kΩ; BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	22,5	25	27,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	31,5	35	38,5	mA
Lowest line current for minimum gain, R11 = 105 kΩ; BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	49,5	55	60,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	81	90	99	mA

DEVELOPMENT SAMPLE DATA

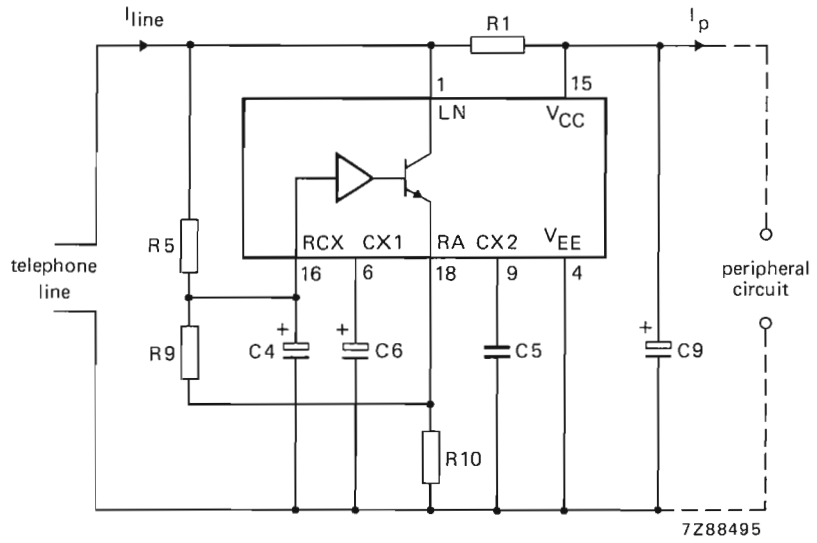


Fig. 3 Supply arrangement.

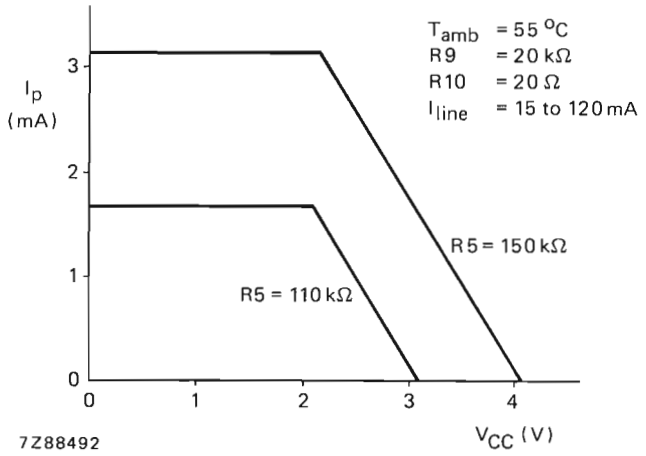


Fig. 4 Maximum current I_p available from V_{CC} for an external circuit.

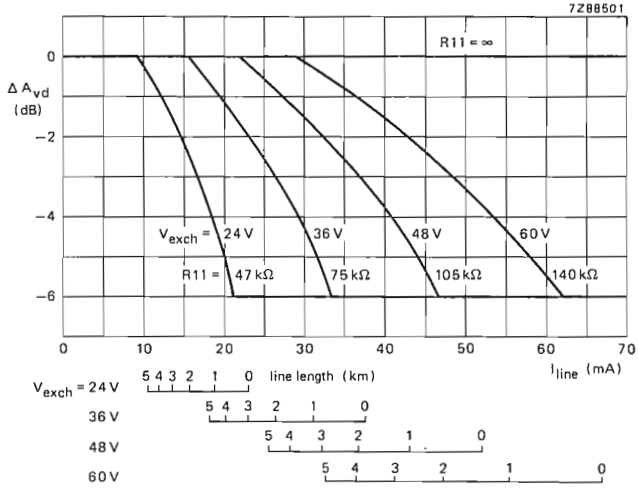


Fig. 5 Gain variation with line current, with R11 as a parameter, and with the BRDG input HIGH, i.e. the circuit optimized for 800 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

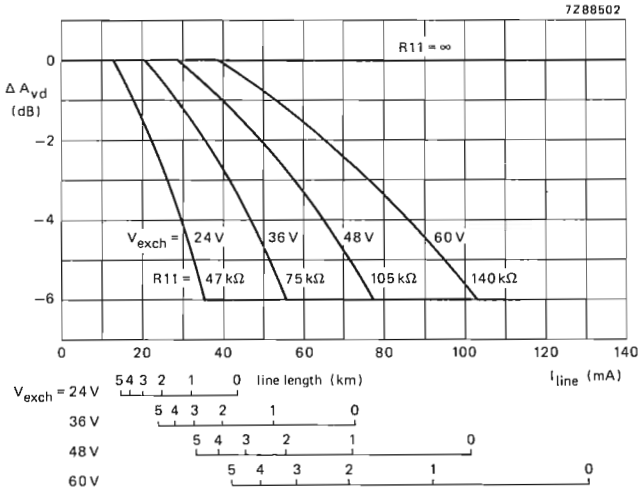


Fig. 6 Gain variation with line current, with R11 as a parameter, and with the BRDG input LOW, i.e. the circuit optimized for 400 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

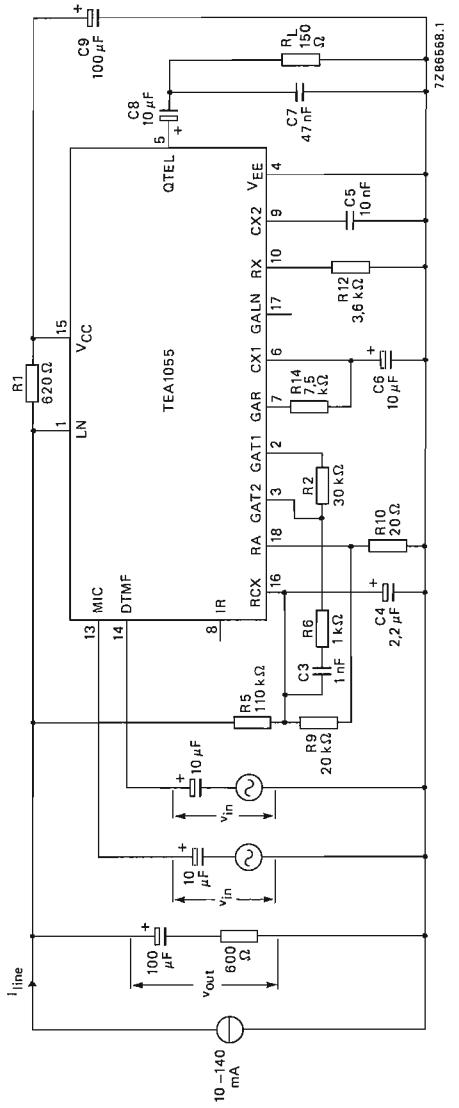


Fig. 7 Test circuit for defining voltage gain of MIC and DTMF inputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the MIC input the MUTE input should be LOW and for measuring the DTMF input MUTE should be HIGH. The input not under test should be open.

DEVELOPMENT SAMPLE DATA

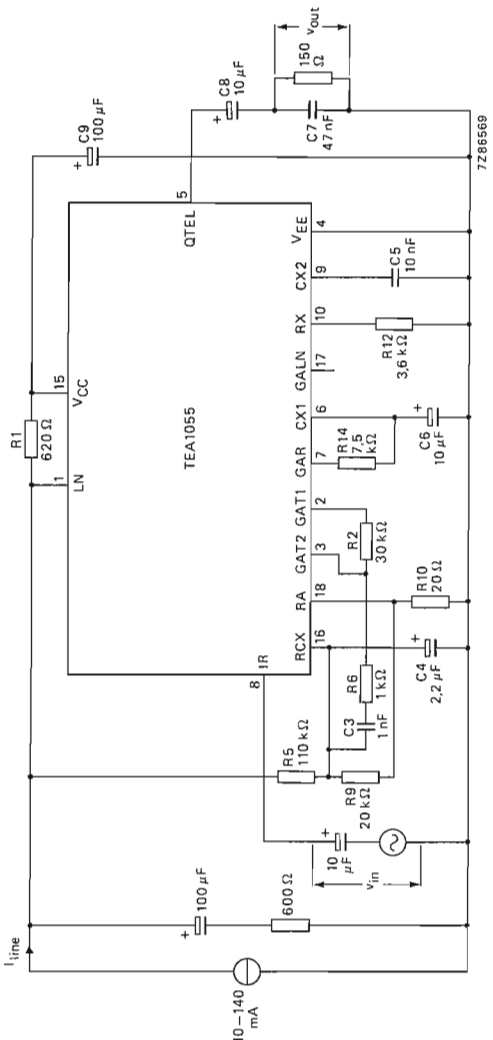


Fig. 8 Test circuit for defining voltage gain of the receiving amplifier. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. The MUTE input should be LOW.

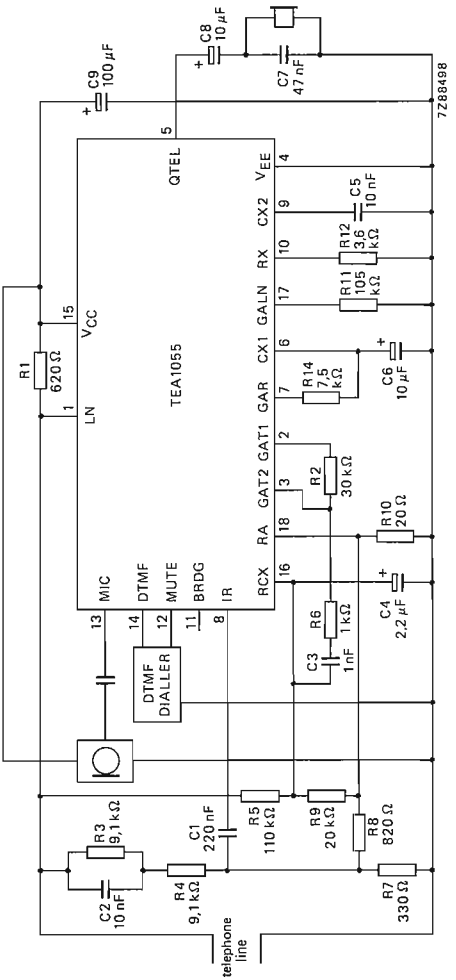
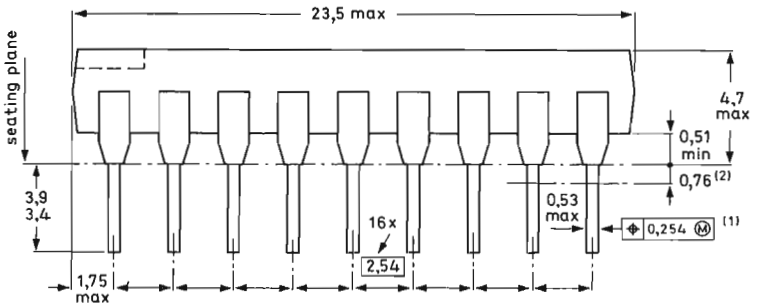
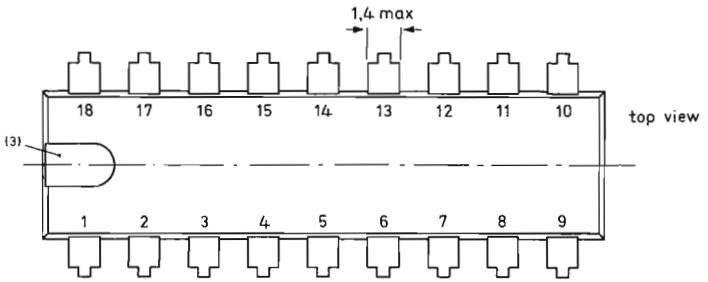


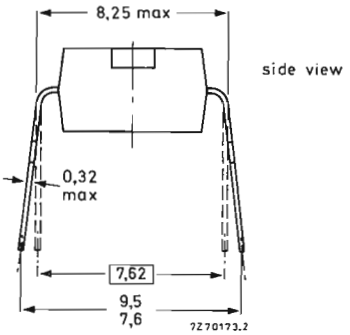
Fig. 9 Typical application of the TEA1055 in an electronic telephone set. The connection to the BRDG input is not shown, see the Functional Description.

APPLICATION INFORMATION SUPPLIED ON REQUEST

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)







⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See next page.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

VERSATILE TELEPHONE TRANSMISSION CIRCUITS WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech and line interface functions required in fully electronic telephone sets. The circuits internally perform electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)
- Asymmetrical high-impedance input for electret microphone (TEA1061)
- DTMF signal input
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on all amplifiers
- Line loss compensation facility, line current dependent
- Gain control adaptable to exchange supply

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ.	4,35	V
Line current operating range	I_{line}	10 to	140	mA
Supply current				
power down input LOW	I_{CC}	typ.	1	mA
power down input HIGH	I_{CC}	typ.	50	μA
Voltage amplification range microphone amplifier				
TEA1060	A_{vd}	44 to	60	dB
TEA1061	A_{vd}	30 to	46	dB
receiving amplifier	A_{vd}	17 to	39	dB
Amplification control range	ΔA_{vd}	typ.	6	dB
Exchange supply voltage range	V_{exch}	24 to	60	V
Exchange feeding bridge resistance range	R_{exch}	400 to	1000	Ω
Operating ambient temperature range	T_{amb}	−25 to	+75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

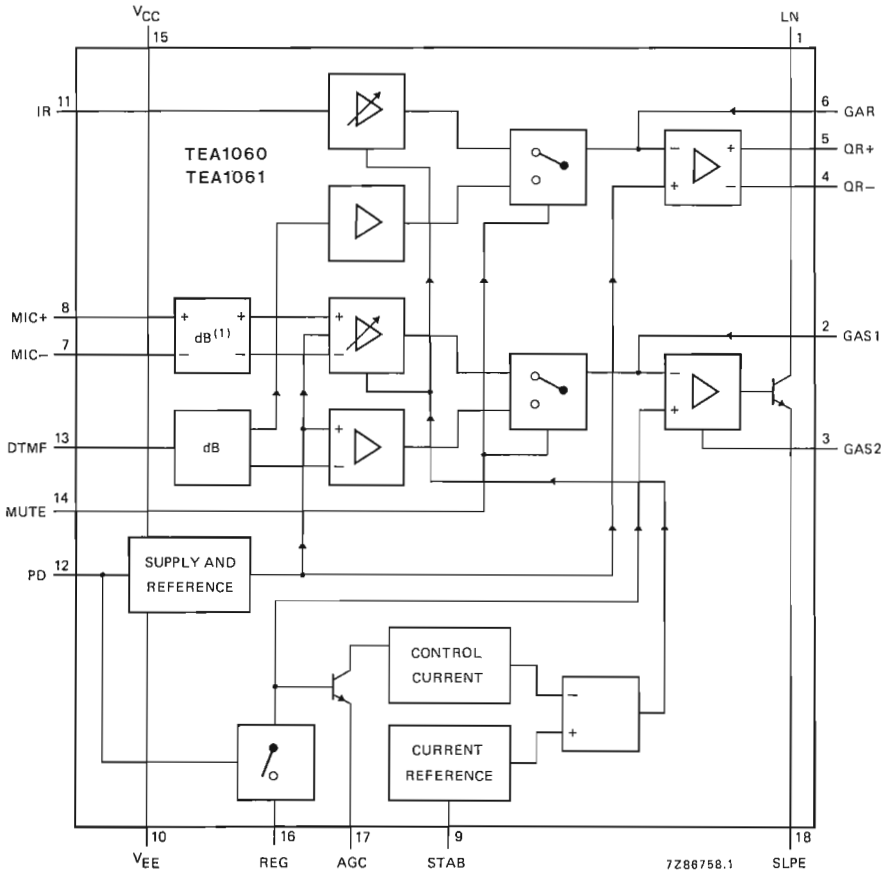


Fig. 1 Block diagram. The blocks marked "dB" are attenuators. The block marked (1) is only present in the TEA1061.

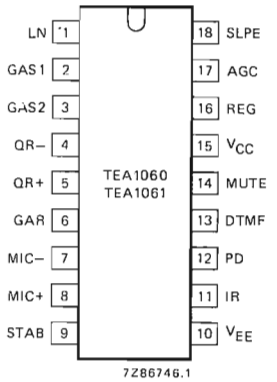


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR−	inverting output; receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC−	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (d.c. resistance) adjustment

DEVELOPMENT SAMPLE DATA

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the d.c. resistance of the subscriber line R_{line} and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current I_{line} exceeds the current I_{CC} + 0,5 mA required by the circuit itself ($I_{CC} \approx 1$ mA), plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0{,}5.10^{-3} - I_p) \times R9.$$

V_{ref} being an internally generated temperature compensated reference voltage of 4,1 V and R9 being an external resistor connected between SLPE and V_{EE}. Under normal conditions $I_{SLPE} \gg I_{CC} + 0{,}5\,mA + I_p$. The static behaviour of the circuit then equals a 4,1 V voltage regulator diode with an internal resistance R9. In the audio-frequency range the dynamic impedance equals R1.

FUNCTIONAL DESCRIPTION (continued)

The current I_p available from V_{CC} for supplying peripheral circuits depends on external components, and on the line current. Figure 4 shows this current for V_{CC} = 3 V min., this being the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC− and gain adjustment pins GAS1 and GAS2

The TEA1060 and TEA1061 have symmetrical microphone inputs.

The TEA1060 is intended for low-sensitivity, low-impedance dynamic or magnetic microphones. Its input impedance is 2 x 4 kΩ and its voltage amplification is typ. 52 dB.

The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 2 x 20 kΩ and its voltage amplification is typ. 38 dB.

The arrangements with the microphone types mentioned are shown in Fig. 5.

The amplification of the microphone amplifier in both types can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 26 dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 6). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB. This makes differential drive possible, which is required for high-impedance dynamic, magnetic and piezoelectric earpieces with load impedances exceeding 450 Ω.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

The amplification of the receiving amplifier can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C6 = 10 x C4 = 1 nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 form AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 7 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input, which reduces the supply current from typ. 1 mA to typ. 50 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the circuit's impedance equals a 4,2 V voltage regulator diode with an internal resistance equal to R9. This results in rectangular current waveforms in pulse dialling and register recall.

When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of R2, R3, R8 and Z_{bal} (see Fig. 10). Maximum compensation is obtained when Z_{bal}/k equals the line impedance Z_{line} as seen by the set (scale factor $k = R_8/R_1$).

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal} equals the line average line impedance.

The anti-side-tone network attenuates the signal from the line. With R8 = 390 Ω and R9 = 20 Ω the attenuation is 32 dB. The attenuation is nearly flat over the audio-frequency range.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line voltage	V_{LN}	max.	13,2 V
Line current			
average	$I_{line(AV)}$	max.	140 mA
non-repetitive (t_{max} = 100 hours)	$I_{line(S)}$	max.	250 mA
non-repetitive peak (t_{max} = 1 ms)	$I_{line(SM)}$	max.	1 A
Voltage on all other pins	V	max.	V_{CC} + 0,7 V
	−V	max.	0,7 V
Total power dissipation	P_{tot}	max.	640 mW
Storage temperature range	T_{stg}	−40 to	+125 °C
Operating ambient temperature range	T_{amb}	−25 to	+75 °C

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)					
Voltage drop over circuit					
at I_{line} = 5 mA	V_{LN}	–	4,15	–	V
at I_{line} = 15 mA	V_{LN}	4,15	4,35	4,55	V
at I_{line} = 100 mA	V_{LN}	–	6,0	7	V
Variation with temperature at I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Supply current					
at V_{CC} = 2,8 V; PD = LOW	I_{CC}	–	0,96	1,25	mA
at V_{CC} = 2,8 V; PD = HIGH	I_{CC}	–	50	–	μA
Microphone inputs MIC+ and MIC−					
Input impedance					
TEA1060	$\lvert z_{is}\rvert$	–	4	–	kΩ
TEA1061	$\lvert z_{is}\rvert$	–	20	–	kΩ
Standard deviation on input impedance	σ	–	12	–	%
Common-mode rejection ratio; TEA1060	k_{CMR}	–	t.b.f.	–	dB
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ					
TEA1060	A_{vd}	51	52	53	dB
TEA1061	A_{vd}	37	38	39	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB

parameter	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF					
Input impedance	$\|z_{is}\|$	–	20	–	kΩ
Standard deviation on input impedance	σ	–	12	–	%
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	25	26	27	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB
Gain adjustment pins GAS1 and GAS2					
Amplification variation with R7, transmitting amplifier	ΔA_{vd}	−8	–	+8	dB
Transmitting amplifier output LN					
Output voltage at I_{line} = 15 mA; d_{tot} = 2%	$V_{LN(rms)}$	1,4	2,3	–	V
d_{tot} = 10%	$V_{LN(rms)}$	–	2,6	–	V
Noise output voltage at I_{line} = 15 mA; R7 = 68 kΩ; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR					
Input impedance	$\|z_{is}\|$	–	20	–	kΩ
Receiving amplifier outputs QR+ and QR−					
Output impedance; single-ended	$\|z_{os}\|$	–	4	–	Ω
Voltage amplification at I_{line} = 15 mA; R4 = 100 kΩ; single-ended; R_L = 300 Ω	A_{vd}	24	25	26	dB
differential; R_L = 600 Ω	A_{vd}	30	31	32	dB
Variation with frequency, at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB
Output voltage at I_p = 0; d_{tot} = 2%; sine-wave drive single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,3	0,38	–	V
single-ended; R_L = 450 Ω	$V_{o(rms)}$	0,4	0,52	–	V
differential; C_L = 47 nF + R_L = 100 Ω; f = 3400 Hz	$V_{o(rms)}$	0,8	1,0	–	V
Noise output voltage at I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve) single-ended; R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential; R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Gain adjustment pin GAR					
Amplification variation with R4, receiving amplifier	ΔA_{vd}	−8	–	+8	dB
MUTE input					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{MUTE}	–	8	15	μA
Reduction of voltage amplification from MIC+ and MIC− to LN at MUTE = HIGH	$-\Delta A_{vd}$	–	70	–	dB
Voltage amplification from DTMF to QR+ or QR− at MUTE = HIGH; single-ended load; R_L = 300 Ω	A_{vd}	–	−18	–	dB
Power-down input PD					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{PD}	–	5	10	μA
Automatic gain control input AGC					
Amplification control range	$-\Delta A_{vd}$	–	6	–	dB
Highest line current for maximum amplification at R6 = 110 kΩ	I_{line}	–	22	–	mA
Lowest line current for minimum amplification at R6 = 110 kΩ	I_{line}	–	60	–	mA

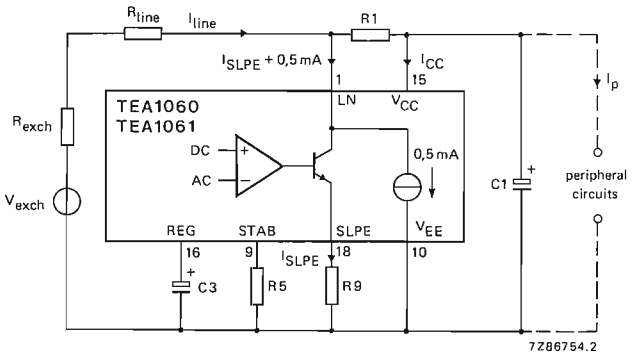


Fig. 3 Supply arrangement.

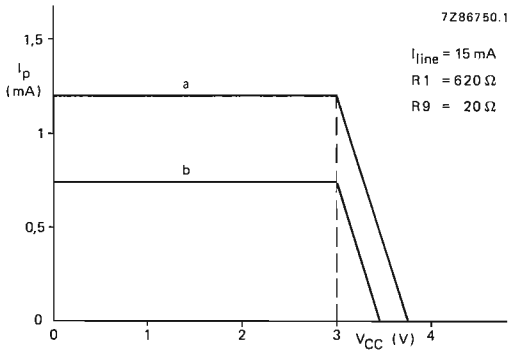


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with $V_{CC} \geqslant 3$ V. Curve "a" is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve "b" is valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$.

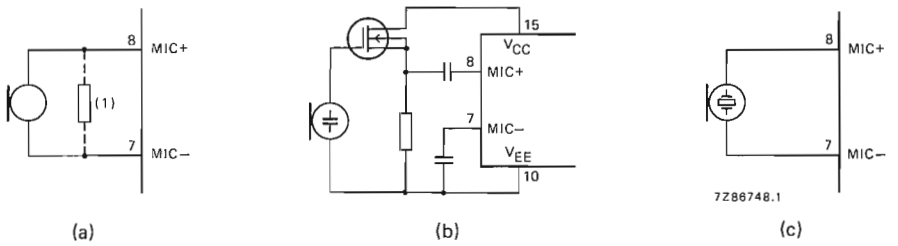


Fig. 5 Alternative microphone arrangements. (a) magnetic or dynamic microphone, TEA1060. The resistor marked (1) may be connected to lower the terminating impedance. (b) electret microphone, TEA1061. (c) piezoelectric microphone, TEA1061.

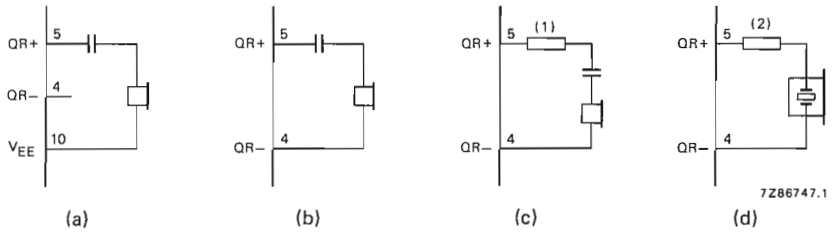


Fig. 6 Alternative receiver arrangements. (a) dynamic telephone with less than 450 Ω impedance. (b) dynamic telephone with more than 450 Ω impedance. (c) magnetic telephone. The resistor marked (1) may be connected to obtain an appropriate acoustic frequency characteristic. (d) piezoelectric telephone. The resistor masked (2) is required to increase the phase margin.

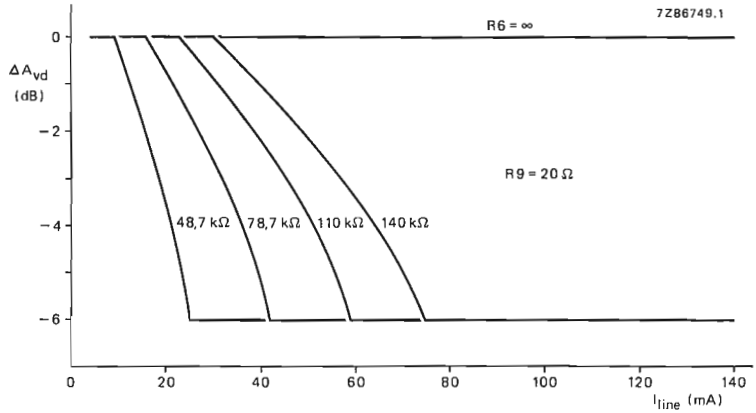


Fig. 7 Variation of amplification with line current, with R6 as a parameter.

Table 1. Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61,9	48,7	X	X
	36	100	78,7	68	60,4
	48	140	110	93,1	82
	60	X	X	120	102

DEVELOPMENT SAMPLE DATA

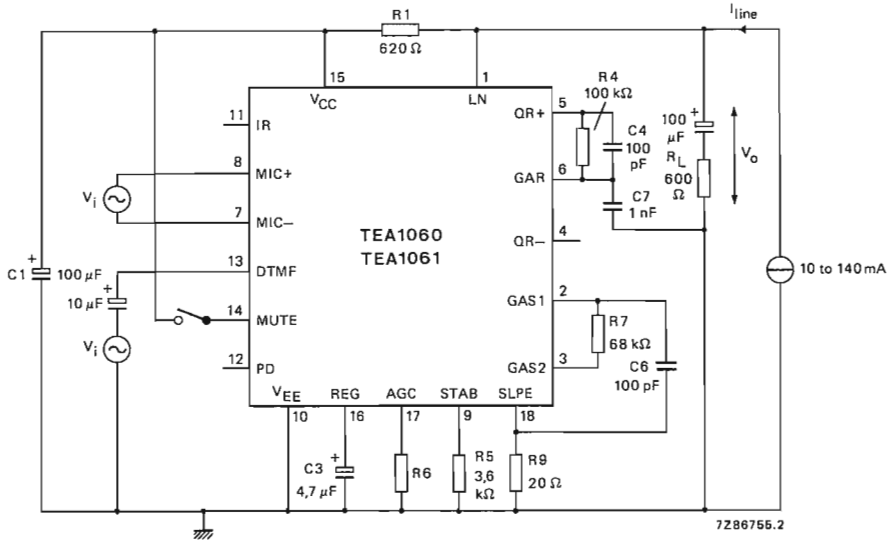


Fig. 8 Test circuit for defining voltage amplification of MIC+, MIC– and DTMF inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. For measuring the amplification from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

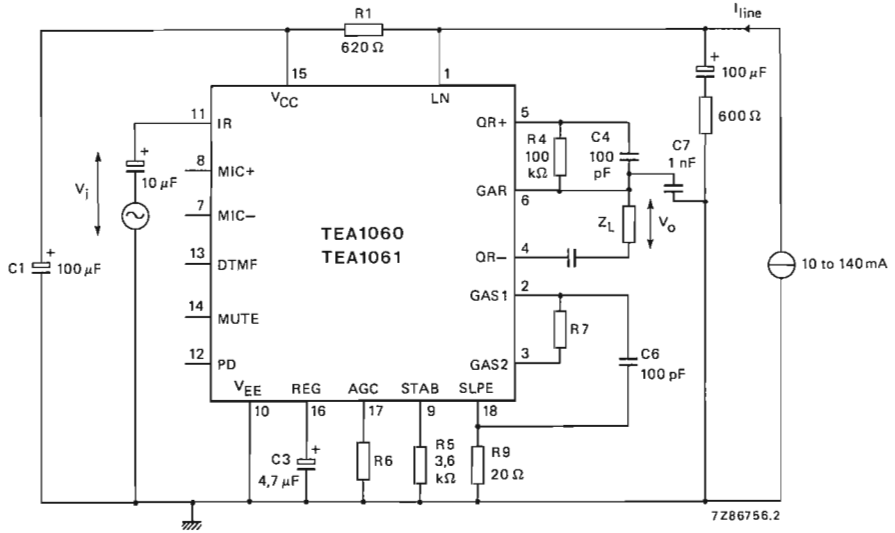


Fig. 9 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

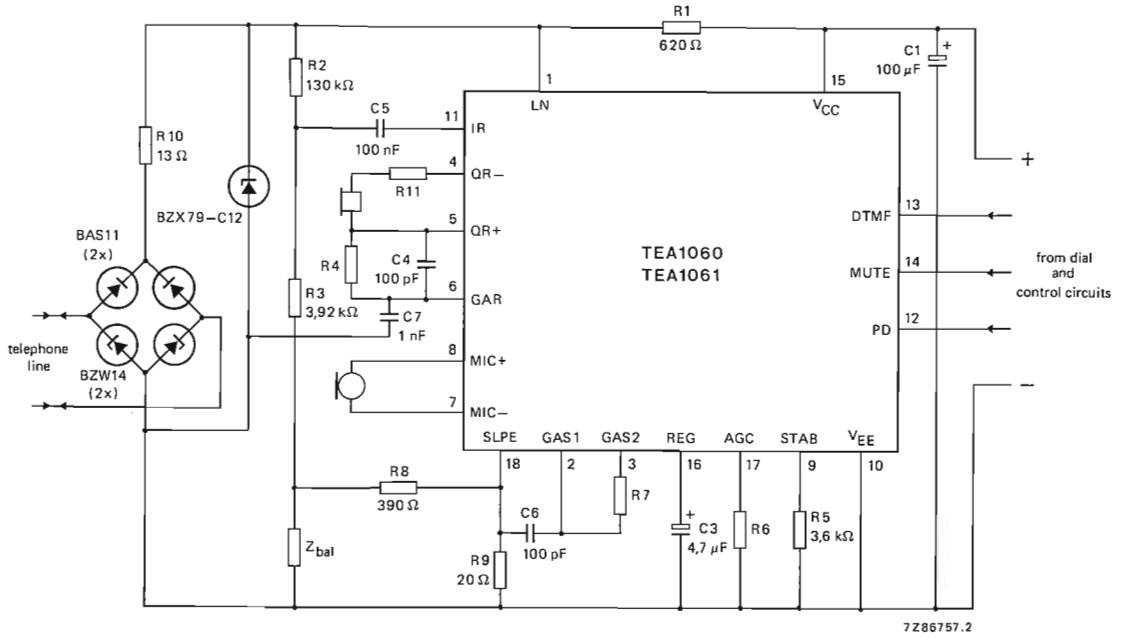


Fig. 10 Typical application of the TEA1060 or TEA1061, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

APPLICATION INFORMATION SUPPLIED ON REQUEST

APPLICATION INFORMATION (continued)

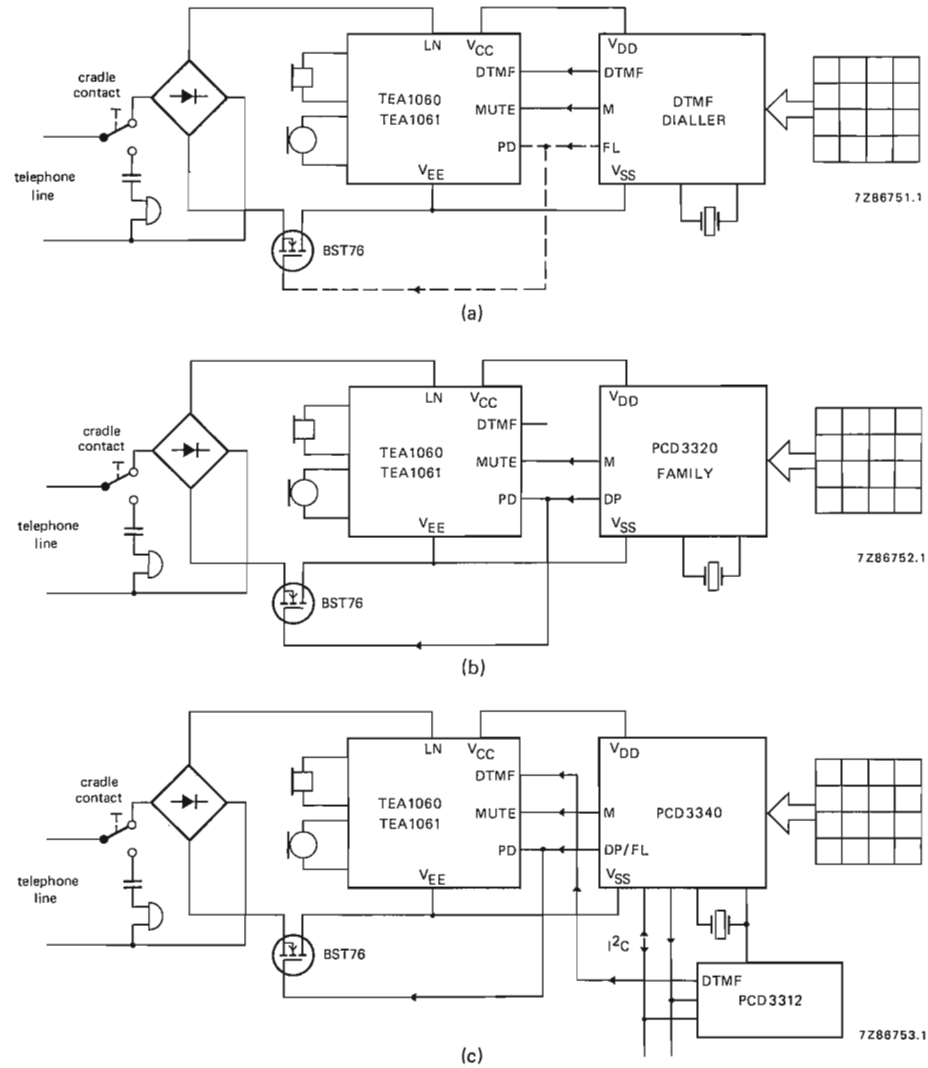
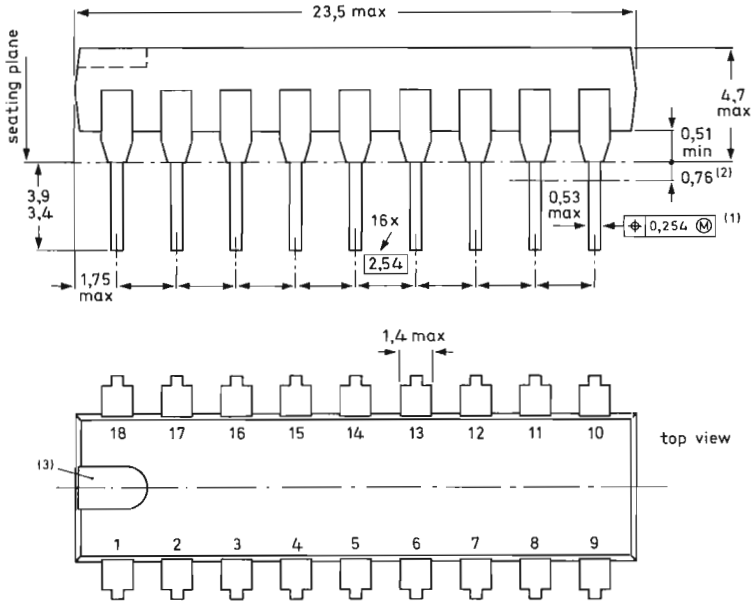
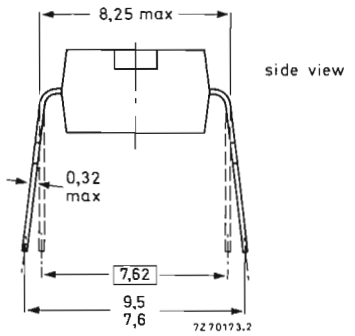


Fig. 11 Typical applications of the TEA1060 or TEA1061 (simplified).

(a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by timed loop break).
(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.
(c) Dual-standard (pulse and DTMF) feature phone with the PCD3340 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C bus.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See next page.

DEVELOPMENT SAMPLE DATA

SOLDERING

1. **By hand**

   Apply the soldering iron below the seating plane (or not more than 2 mm above it).
   If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. **By dip or wave**

   The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. **Repairing soldered joints**

   The same precautions and limits apply as in (1) above.

VERSATILE TELEPHONE TRANSMISSION CIRCUITS

GENERAL DESCRIPTION

The TEA1062 and TEA1063 are bipolar integrated circuits performing all speech and line interface functions required in fully electronic telephone sets. The devices can be installed in the handset to facilitate two-wire connection to the dial and control circuits mounted in the base of the telephone set.

Features

- Voltage regulator with adjustable static resistance
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1062)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1063)
- Asymmetrical high-impedance input for electret microphone (TEA1063)
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on all amplifiers
- Line loss compensation facility, line current dependent
- Gain control adaptable to exchange supply

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ. 3,75	V
Line current operating range	I_{line}	10 to 140	mA
Supply current	I_{CC}	typ. 1	mA
Voltage amplification range			
microphone amplifier			
TEA1062	A_{vd}	44 to 60	dB
TEA1063	A_{vd}	30 to 46	dB
receiving amplifier	A_{vd}	17 to 39	dB
Amplification control range	ΔA_{vd}	typ. 6	dB
Exchange supply voltage range	V_{exch}	24 to 60	V
Exchange feeding bridge resistance range	R_{exch}	400 to 1000	Ω
Operating ambient temperature range	T_{amb}	−25 to + 75	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

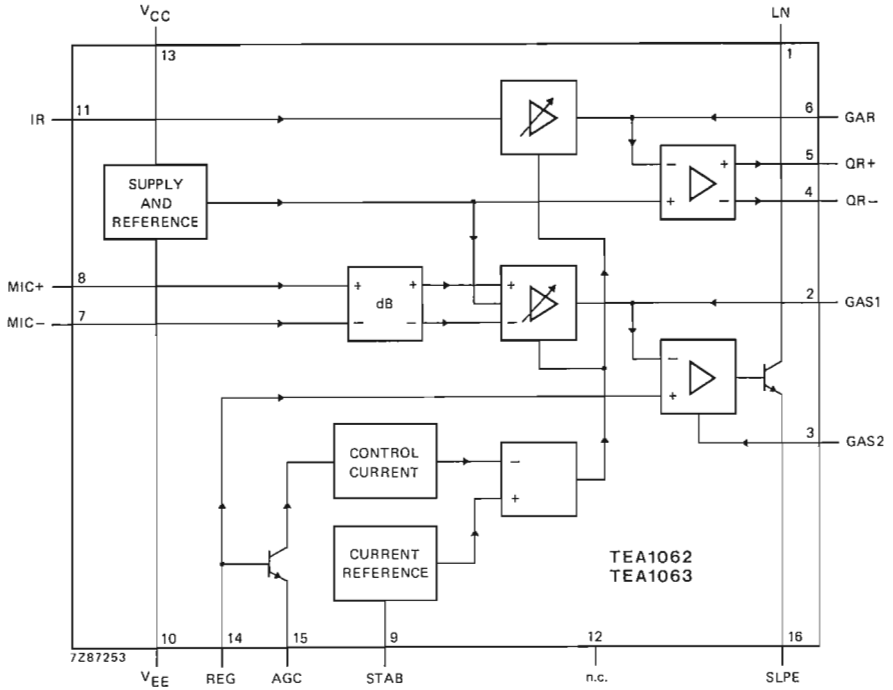


Fig. 1 Block diagram. The block marked "dB" is an attenuator which is present only in the TEA1063.

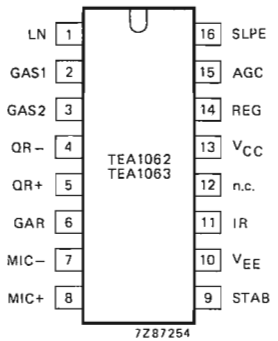


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output; receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	n.c.	not connected
13	V_{CC}	positive supply decoupling
14	REG	voltage regulator decoupling
15	AGC	automatic gain control input
16	SLPE	slope (d.c. resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its associated dial and control circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be applied to a FET source follower to be used as an impedance converter for an electret microphone.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the d.c. resistance of the subscriber line R_{line} and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current I_{line} exceeds the current I_{CC} required by the circuit itself, i.e. about 1 mA, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{LN} \times R9 = V_{ref} + (I_{line} - I_{CC}) \times R9,$$

V_{ref} being an internally generated temperature compensated reference voltage of 3,45 V and R9 being an external resistor connected between SLPE and V_{EE}. Under normal conditions $I_{LN} \approx I_{CC}$. The static behaviour of the circuit then equals a 3,45 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1.

Microphone inputs MIC+ and MIC− and gain adjustment pins GAS1 and GAS2

The TEA1062 and TEA1063 have differential microphone inputs.

The TEA1062 is intended for low-sensitivity low-impedance dynamic or magnetic microphones. Its input impedance is 2 x 4 kΩ and its voltage amplification is typ. 52 dB.

The TEA1063 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 2 x 20 kΩ and its voltage amplification is typ. 38 dB.

The arrangements with the microphone types mentioned are shown in Fig. 4.

The amplification of the microphone amplifier in both types can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 5). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB. This makes differential drive possible for high-impedance dynamic, magnetic and piezoelectric earpieces with load impedances exceeding 180 Ω.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

FUNCTIONAL DESCRIPTION (continued)

The amplification of the receiving amplifier can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

An external capacitor C4 of 100 pF between QR+ and GAR is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 6 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required, AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of R2, R3, R8 and Z_{bal} (see Fig. 9). Maximum compensation is obtained when Z_{bal} equals the line impedance Z_{line} as seen by the set.

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal} approaches the average line impedance.

The anti-side-tone network attenuates the signal from the line. With R8 = 620 Ω and R9 = 20 Ω, the attenuation is 29,1 dB. The attenuation is flat over the audio frequency range.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line supply voltage	V_{LN}	max.	15 V
Line current			
average	$I_{line(AV)}$	max.	140 mA
non-repetitive (t_{max} = 100 hours)	$I_{line(S)}$	max.	250 mA
non-repetitive peak (t_{max} = 1 ms)	$I_{line(SM)}$	max.	1 A
Voltage on all other pins	V	max.	V_{CC} + 0,7 V
	−V	max.	0,7 V
Total power dissipation	P_{tot}	max.	640 mW
Storage temperature range	T_{stg}		−40 to + 125 °C
Operating ambient temperature range	T_{amb}		−25 to + 75 °C

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)					
Voltage drop over circuit					
at I_{line} = 5 mA	V_{LN}	–	3,55	–	V
at I_{line} = 15 mA	V_{LN}	3,55	3,75	3,95	V
at I_{line} = 100 mA	V_{LN}	–	5,4	6,2	V
Variation with temperature	$\Delta V_{LN}/\Delta T$	−2	0	+ 2	mV/K
Supply current at V_{CC} = 2,8 V	I_{CC}	–	0,96	1,25	mA
Microphone inputs MIC+ and MIC−					
Input impedance					
TEA1062	$\lvert z_{is} \rvert$	–	4	–	kΩ
TEA1063	$\lvert z_{is} \rvert$	–	20	–	kΩ
Standard deviation on input impedance	σ	–	12	–	%
Common-mode rejection ratio; TEA1062	k_{CMR}	–	t.b.f.	–	dB
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ					
TEA1062	A_{vd}	51	52	53	dB
TEA1063	A_{vd}	37	38	39	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	± 0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,5	–	dB
Gain adjustment pins GAS1 and GAS2					
Amplification variation with R7, transmitting amplifier	ΔA_{vd}	−8	–	+ 8	dB
Transmitting amplifier output LN					
Output voltage at I_{line} = 15 mA;					
d_{tot} = 2%	$V_{LN(rms)}$	1,2	1,8	–	V
d_{tot} = 10%	$V_{LN(rms)}$	–	2,1	–	V
Noise output voltage at I_{line} = 15 mA; R7 = 68 kΩ; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR					
Input impedance	$\lvert z_{is} \rvert$	–	20	–	kΩ

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Receiving amplifier outputs QR+ and QR−					
Output impedance; single-ended	$\lvert z_{os} \rvert$	–	15	–	Ω
Voltage amplification at I_{line} = 15 mA; R4 = 100 kΩ;					
single-ended; R_L = 150 Ω	A_{vd}	24	25	26	dB
differential; R_L = 450 Ω	A_{vd}	30	31	32	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	± 0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta A_{vd}/\Delta T$	–	± 0,5	–	dB
Output voltage at d_{tot} = 2%; sine-wave drive					
single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,25	0,3	–	V
differential; R_L = 450 Ω	$V_{o(rms)}$	0,45	0,55	–	V
differential; C_L = 47 nF; f = 3400 Hz	$V_{o(rms)}$	0,6	0,75	–	V
Noise output voltage at I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve)					
single-ended; R_L = 150 Ω	$V_{no(rms)}$	–	50	–	μV
differential; R_L = 450 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment pin GAR					
Amplification variation with R4, receiving amplifier	ΔA_{vd}	−8	–	+ 8	dB
Automatic gain control input AGC					
Amplification control range	$-\Delta A_{vd}$	–	6	–	dB
Highest line current for maximum amplification at R6 = 100 kΩ	I_{line}	–	23	–	mA
Lowest line current for minimum amplification at R6 = 100 kΩ	I_{line}	–	58	–	mA

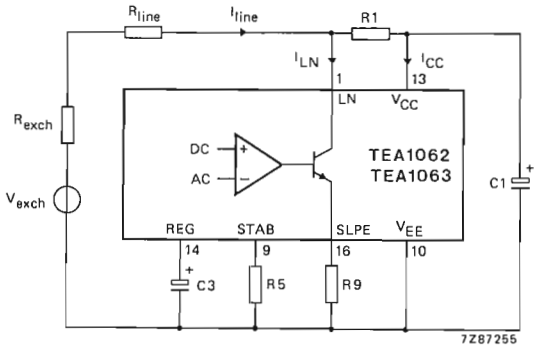


Fig. 3 Supply arrangement.

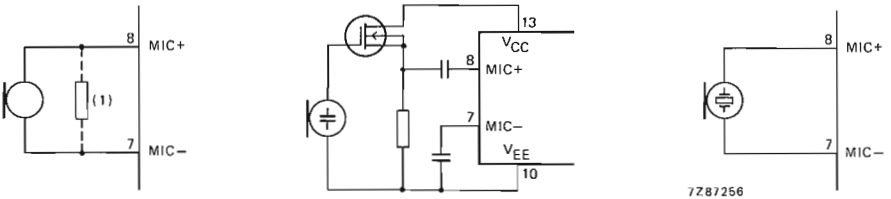


Fig. 4 Alternative microphone arrangements: (a) magnetic or dynamic microphone, TEA1062 (the resistor marked (1) may be connected to lower the terminating impedance); (b) electret microphone, TEA1063; (c) piezoelectric microphone, TEA1063.

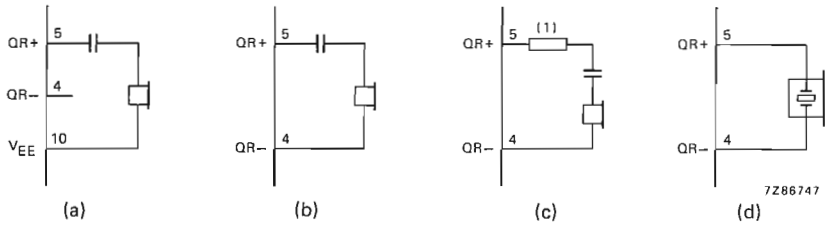


Fig. 5 Alternative receiver arrangements: (a) dynamic telephone with less than 180 Ω impedance; (b) dynamic telephone with more than 180 Ω impedance; (c) magnetic telephone (the resistor marked (1) may be connected to obtain an appropriate acoustic frequency characteristic); (d) piezoelectric telephone.

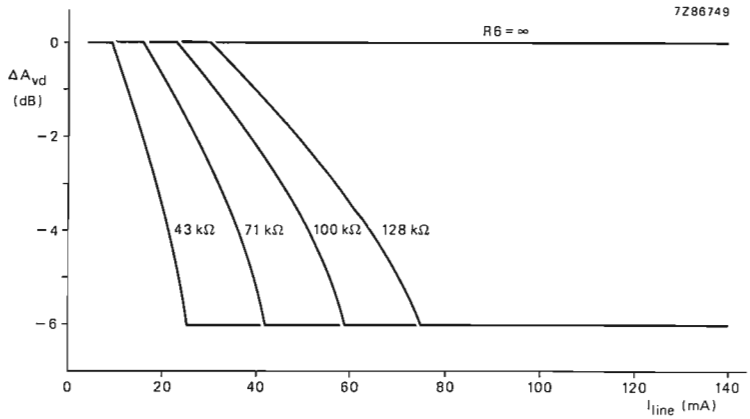


Fig. 6 Variation of amplification with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for common values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	55	43	X	X
	36	91	71	60	52
	48	128	100	84	71
	60	X	X	107	92

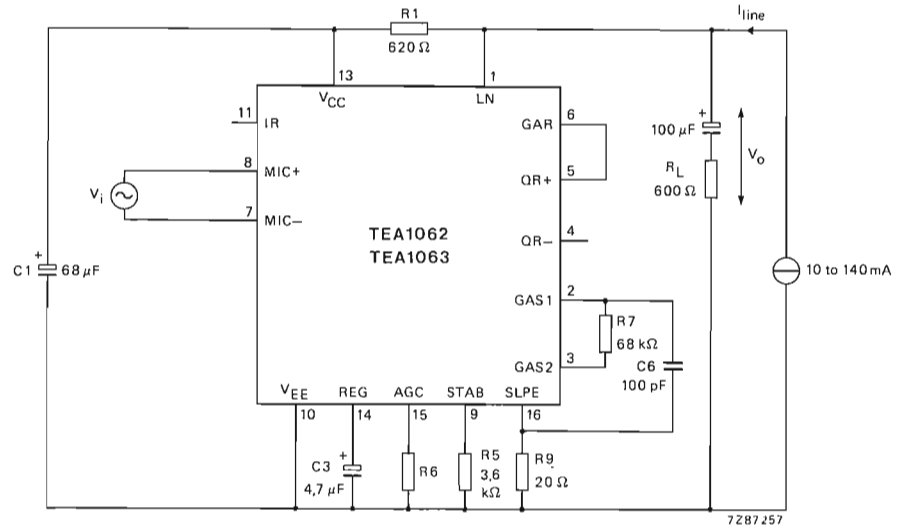


Fig. 7 Test circuit for defining voltage amplification of MIC+, MIC– inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. Inputs not under test should be open circuit.

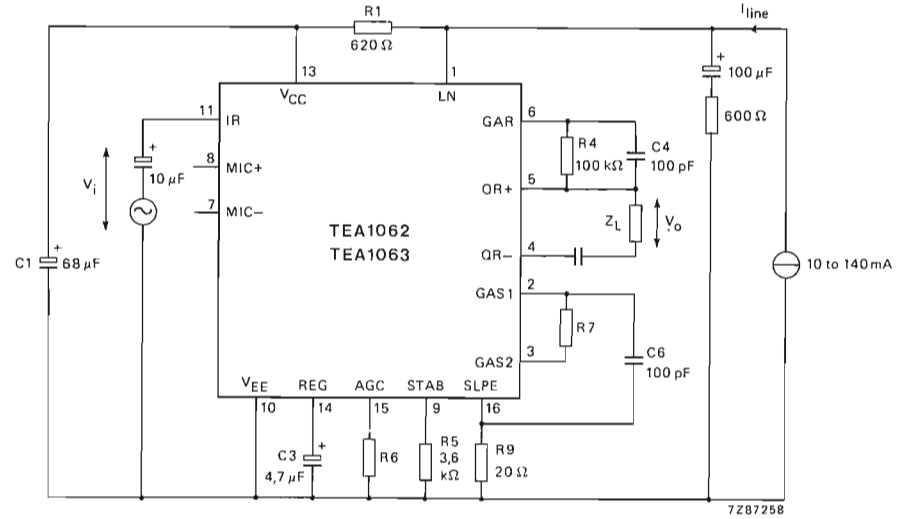


Fig. 8 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

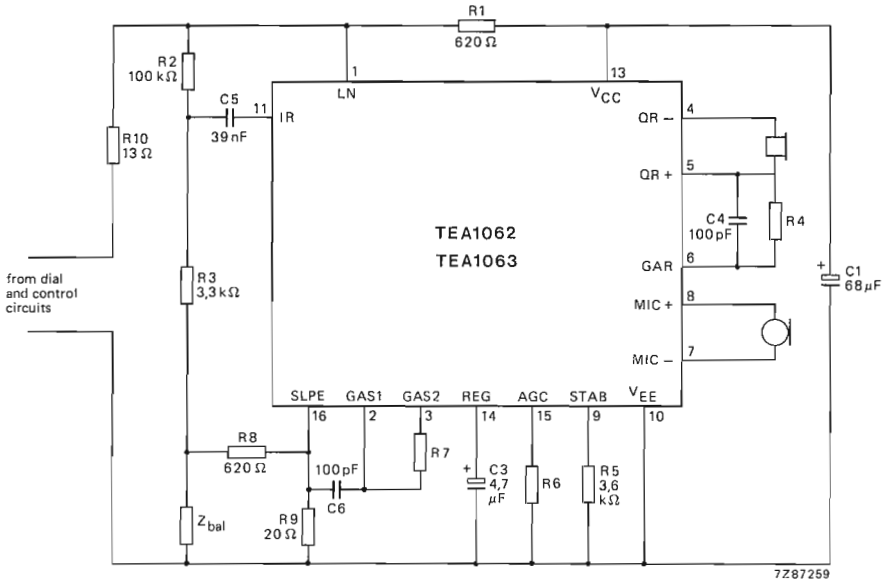
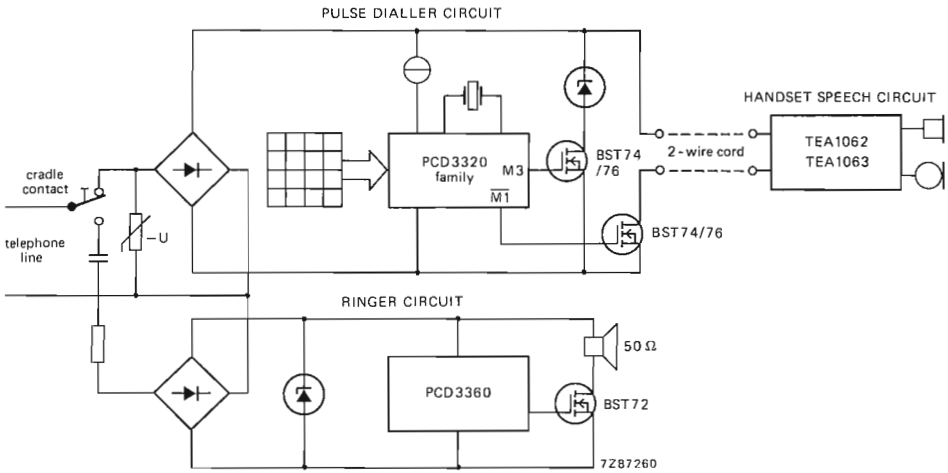
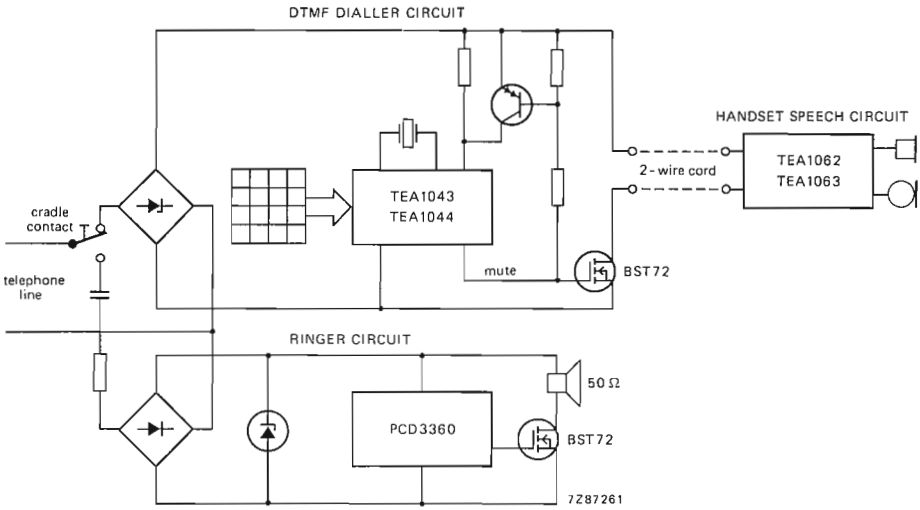


Fig. 9 Typical application of the TEA1062 or TEA1063, shown here with a piezoelectric earpiece. Resistor R10 limits the current into the circuit during line transients. Voltage limitation resulting from transients depends on the dialling system and is not indicated.

APPLICATION INFORMATION SUPPLIED ON REQUEST



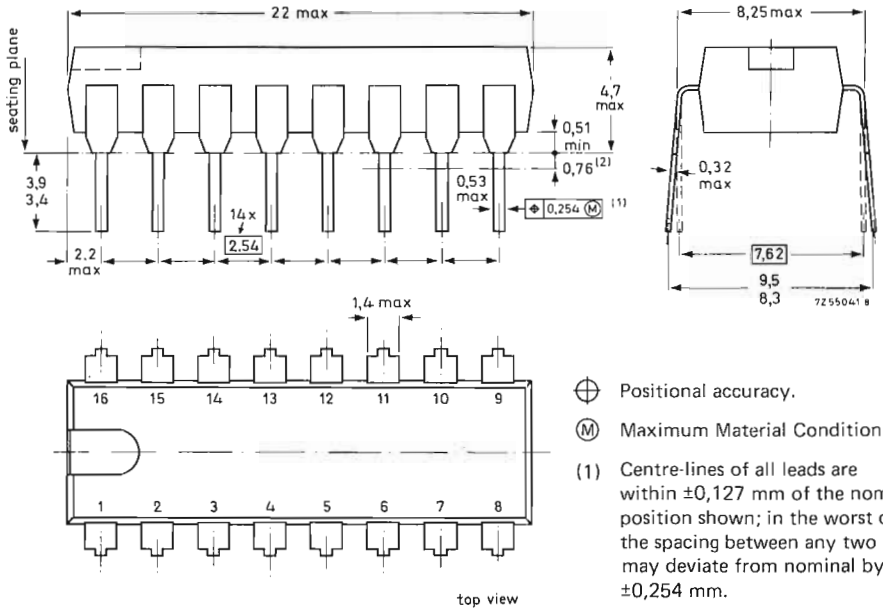
(a)



(b)

Fig. 10 Typical applications (simplified) of the TEA1062 or TEA1063: (a) basic pulse dial set with one of the PCD3320 family of C-MOS interrupted current-loop dialling circuits; (b) basic DTMF set with TEA1043/TEA1044 bipolar DTMF dialler.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

DTMF/speech transmission combination

DTMF/SPEECH TRANSMISSION INTEGRATED CIRCUIT FOR TELEPHONE APPLICATIONS

This integrated circuit is a dual-tone multi-frequency (DTMF) generator and a speech transmission circuit on a single chip. It supplies frequency combinations in accordance with CCITT recommendations for use in push-button telephones. It can be operated with a single contact keyboard or via a direct interface with a microcomputer. I^2L technology allows digital and analogue functions to be implemented on the same chip.

The speech-transmission part incorporates microphone and telephone amplifiers, anti-sidetone and line adaption. The microphone inputs, suitable for different types of transducers, are symmetrical to allow long cable connections with good immunity against radio-frequency interferences.

The logic inputs contain an interface circuit to guarantee well defined states and on and off resistance of the keyboard contacts.

The circuit features:
- stabilized DTMF levels to be set externally
- wide operating range of line current and temperature
- no individual DTMF level adjustments required
- microcomputer compatible logic inputs
- gain setting for microphone and receiver amplifiers
- internally generated electronic muting
- low spreads on amplifier gains
- low number of external components

QUICK REFERENCE DATA

Line voltage	V_L	typ. 4,8	V
Line current	I_L	10 to 120	mA
Adjustable dynamic resistance	R_i	600 to 900	Ω
Microphone signal amplification	A_M	typ. 50	dB
Telephone signal amplification	A_T	typ. 20	dB
DTMF tone levels (adjustable)			
lower frequency	V_{LG}	max. −6	dBm
higher frequency	V_{HG}	max. −4	dBm
Operating temperature range	T_{amb}	−25 to +85	°C

PACKAGE OUTLINES

TEA1046P : 24-lead DIL, plastic (SOT-101).
TEA1046D: 24-lead DIL, ceramic (SOT-94).

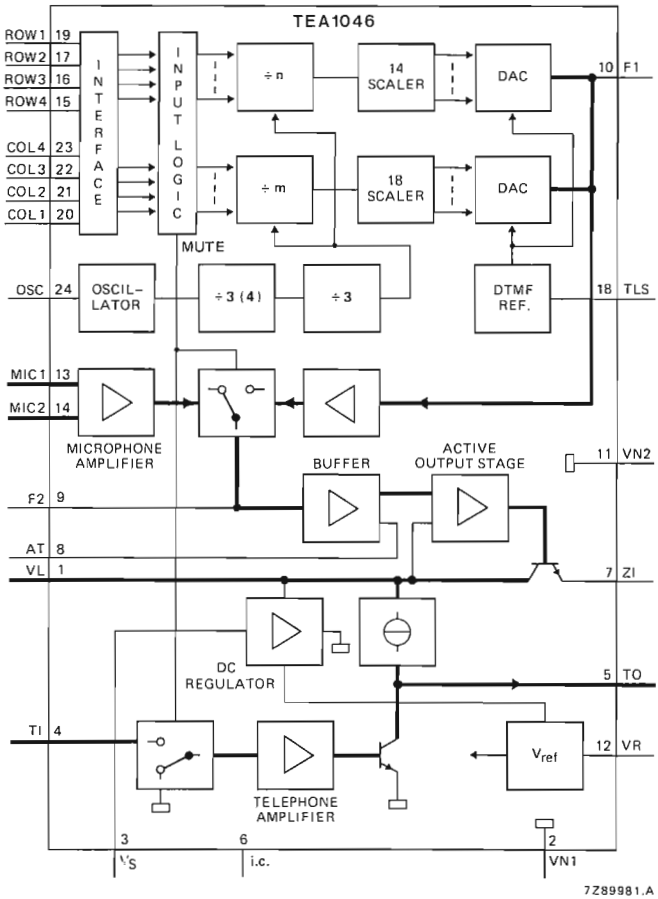


Fig. 1 Functional block diagram.

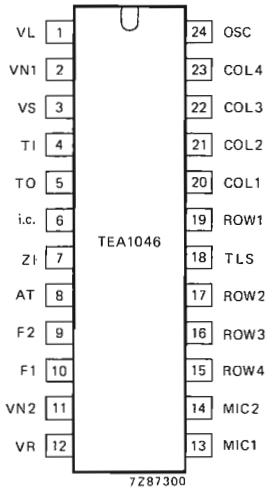


Fig. 2 Pinning diagram.

PINNING

1	VL	positive line-voltage
2	VN1	negative line-voltage
3	VS	voltage stabilizer filter
4	TI	telephone amplifier input
5	TO	telephone amplifier output
6	i.c.	internally connected
7	ZI	impedance setting input
8	AT	anti-sidetone output
9	F2	second filter
10	F1	first filter
11	VN2	negative line voltage
12	VR	reference voltage output
13	MIC1	microphone input (pos.)
14	MIC2	microphone input (neg.)
15	ROW4	row input 941 Hz/BCD input
16	ROW3	row input 852 Hz/BCD input
17	ROW2	row input 770 Hz/BCD input
18	TLS	DTMF level setting
19	ROW1	row input 697 Hz/BCD input
20	COL1	column input 1209 Hz/mute input
21	COL2	column input 1336 Hz/mute input
22	COL3	column input 1477 Hz/enable input
23	COL4	column input 1633 Hz/mute input
24	OSC	oscillator input

FUNCTIONAL DESCRIPTION

Voltage regulator (Fig. 3)

Different line lengths and feeding bridge resistances of the exchange cause a large line current range to supply this circuit. As all functions on this chip are working within a total current of 10 mA, the rest of the line current is shunted by the voltage regulator circuit. It regulates the voltage drop over the circuit on a nominal level of 4,8 V.

The capacitor connected to input VS provides a low-pass filter function to avoid influence of the audio signals on the line.

The static behaviour of the voltage regulator is expressed by:

$$V_L = V_o + (I_L - I_i)\ R13$$

where V_o = 4,8 V at T_a = 25 °C and R13 = 5 Ω, I_i = 10 mA.

The dynamic impedance of the regulator is equivalent to a resistor in series with a simulated inductor:

$$Zr\ (\omega) = R_{eq} + j\omega L_{eq}$$

where R_{eq} = R13 = 5 Ω
$L_{eq} \approx 5$ H (C_{VS} = 68 μF).

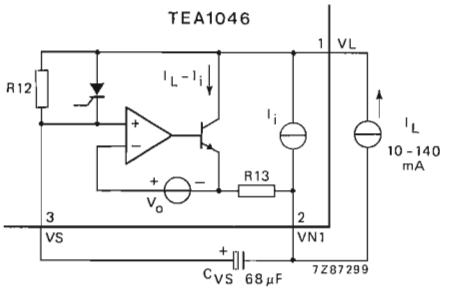


Fig. 3 Voltage regulator principle.

By connecting a resistor parallel to R12 the d.c. level (V_L) can be decreased. A resistor parallel C_{VS} increases the level (see Fig. 3). All this with respect to limited values. The shunt regulator contains a thyristor which short-circuits R12 for a short period during the switch-on time. This reduces the overshoot voltage to only 1 V above the level set by the regulator.

Active output stage

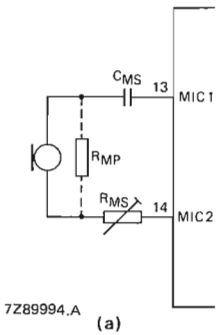
The amplifier consists of a voltage to current converter with a class-A output stage. Because of the feedback from the line to the input the circuit acts as a dynamic resistance (R_a). This resistance can be adjusted by the external resistor R_{ZI} and the value can be found by:

$$R_a = 8{,}93 \times R_{ZI}\ (\Omega)$$

The total dynamic resistance R_i equals R_a parallel with the resistance R_P of all other circuits parts, which value is approximately 7 kΩ.
With $R_{ZI} = 75\ \Omega$, $R_a = 670\ \Omega$ and $R_i = 610\ \Omega$.
For $R_{ZI} = 120\ \Omega$, $R_a = 1070\ \Omega$ and $R_i = 900\ \Omega$.

Microphone amplifier

Pins 13 and 14 respectively are the non-inverting and inverting inputs for the microphone. The purely symmetrical inputs are suitable for low ohmic dynamic or magnetic capsules. The input impedance equals 4 kΩ. The voltage amplification from microphone input to pin 1 (VL) is 50 dB and if a lower gain is required the attenuation for a series resistor R_{MS} will be:

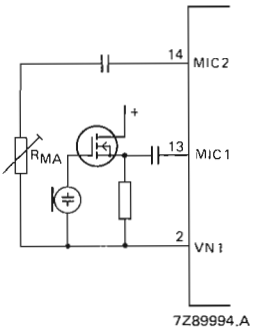


$$\frac{A_M(R_{MS} \neq 0)}{A_M(R_{MS} = 0)} = \frac{4}{4 + R_{MS}} \qquad (R_{MS} \text{ in k}\Omega)$$

$$A_M = \left|\frac{V_L}{V_M}\right|$$

Fig. 4 Symmetrical microphone connection. Resistor R_{MP} may be used to lower the microphone termination resistance.

The microphone amplifier also has an excellent behaviour for connection of an electret microphone with built in FET-source follower. In this condition pin 14 is decoupled for a.c. and the amplifier is driven at pin 13. The input impedance in this asymmetrical mode is 22 kΩ. If attenuation of the amplification is required the value of R_{MA} is given by:



(b)

$$\frac{A_M(R_{MA} \neq 0)}{A_M(R_{MA} = 0)} = \frac{22 + R_{MA}}{22 + 11R_{MA}} \quad (R_{MA} \text{ in k}\Omega)$$

$$A_M = \left| \frac{V_L}{V_{MIC1}} \right|$$

Fig. 5 Electret microphone circuit.

DEVELOPMENT SAMPLE DATA

Telephone amplifier and anti-sidetone network

This amplifier is a non-inverting fixed feedback amplifier with a class-A output stage. The gain is fixed and measures 20 dB from pin 4 (TI) to pin 5 (TO). The output is intended to drive capsules Z_T of nom. 350 Ω. For Z_T smaller than 350 Ω the maximum output voltage swing is determined by the bias current of 3,5 mA and Z_T. For Z_T greater than 350 Ω the maximum voltage swing is determined internally. The received line signal is attenuated by the anti-sidetone network and can be adjusted by R_{AT}. The amplification from the line to the telephone output is given by:

$$A_T = 10 \frac{R_{AT}}{R_{AT} + Z_S} \times \frac{Z_T}{Z_T + R_O} \qquad \text{(see Fig. 14)}$$

Z_S is the impedance of the anti-sidetone network
Z_T is the capsule impedance
R_O is the amplifier output resistance

Optimum side-tone suppression is obtained as Z_S (R_{A1}, R_{A2} and C_A) equals

$$Z_S = K \frac{Z_L \times R_i}{Z_L + R_i}$$

Z_L = line terminating impedance
R_i = output stage impedance // passive circuit impedance
K = 237

In the application of Fig. 14 the network is optimized for 5 km of twisted copper wire (ϕ0,5 mm) cable with a d.c. resistance of 176 Ω/km. The side-tone suppression in the range from 0 – 10 km is at least 10 dB compared with the case when no compensation is applied.

Keyboard inputs

Inputs for the logic control are compatible with different types of keyboard. Using a keyboard, tone combinations are generated:

- by connecting one of row inputs to one of the column inputs by means of a single switch of the matrix.
- or by applying a dual contact keyboard having its common row contact tied to ground and the common column contact tied to VR.

An anti-bounce circuit eliminates the switch bounce for up to 2 ms. Two key roll-over is provided by blocking other inputs as soon as one key is pressed. Single tones can be generated if the column input is connected to VR or the row input to ground. The inputs for the keyboard connections can be used for direct connection to a microcomputer. If the column inputs are interconnected and made HIGH (= VR) the row inputs are changed to another mode, allowing the circuit to be driven by 4-bit data plus an enable signal. In this mode, it is also possible to connect a separate mute enable signal on inputs COL1, 2 and 4 and a tone enable input on COL3.

Truth table microcomputer mode

row				column		tones Hz	symbol	mute
1	2	3	4	1, 2, 4	3			
H	H	H	H	L	L	–	–	off
X	X	X	X	H	L	–	–	on
H	H	H	H	H	H	697/1209	1	on
H	H	H	L	H	H	697/1336	2	on
H	H	L	H	H	H	697/1477	3	on
H	H	L	L	H	H	697/1633	A	on
H	L	H	H	H	H	770/1209	4	on
H	L	H	L	H	H	770/1336	5	on
H	L	L	H	H	H	770/1477	6	on
H	L	L	L	H	H	770/1633	B	on
L	H	H	H	H	H	852/1209	7	on
L	H	H	L	H	H	852/1336	8	on
L	H	L	H	H	H	852/1477	9	on
L	H	L	L	H	H	852/1633	C	on
L	L	H	H	H	H	941/1209	*	on
L	L	H	L	H	H	941/1336	0	on
L	L	L	H	H	H	941/1477	#	on
L	L	L	L	H	H	941/1633	D	on

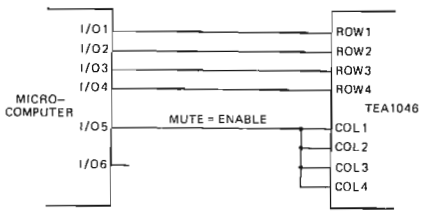
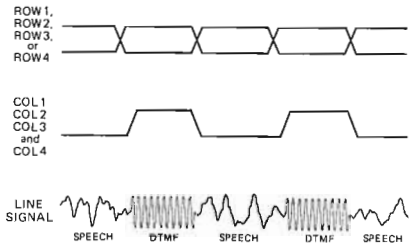


Fig. 6 Microcomputer mode.
All column inputs interconnected.



(a)

Fig. 7 Tone/speech waveform in circuit diagram Fig. 6.

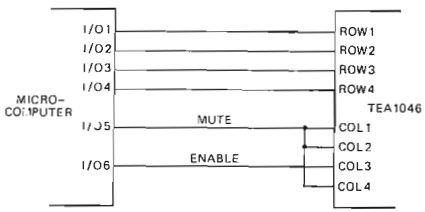
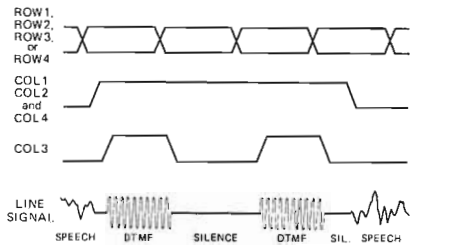


Fig. 8 Microcomputer mode.
Column inputs COL1, 2 and 3 interconnected.



(b)

Fig. 9 Tone/speech waveform in circuit diagram Fig. 8.

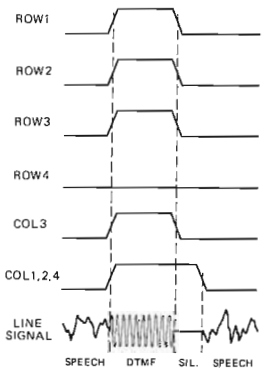


Fig. 10 Waveform tones 697/1336 Hz (dialling number 2).

Dial tone generator

The crystal oscillator frequency is twelve or nine times the clock frequency i.e. 4,782 720 MHz or 3,579 545 MHz (mask option). The CCITT recommends that the tones should be within 1,5% of the specified frequencies. Many authorities however require a closer tolerance. The application using a crystal of 4,78 MHz gives a maximum dividing error of 0,11% whilst for an application with a 3,58 MHz crystal the error is 0,25% maximum.

The output from the dividers for the higher and the lower frequency tones are symmetrical square-wave pulses which contain considerable odd-numbered harmonics. The lower order odd numbered harmonics (11th and less) are eliminated by synthesising the tone frequencies as crude stepped sinewave approximations. Each half cycle of the tone waveform comprises seven discrete amplitudes for the higher frequency tone. Each amplitude increment is generated by switching on and off an individual current source for the duration of each step of the sinewave. The frequency of the tones is varied by changing the duration of each step. This circuit allows the connecting of two low-pass first order filters to pins 9 and 10 if CEPT 203 recommendations have to be achieved.

The second filter is also used for filtering the microphone signal. If lower requirements for the distortion can be applied the filter at pin 10 can be deleted. In that case the filter at pin 9 must have a lower cut-off frequency (1800 Hz) to achieve a correct pre-emphasis since the roll-off of the filters is compensated internally.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150 mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	850 mA
Operating ambient temperature range	T_{amb}	−25 to	+85 °C
Storage temperature range	T_{stg}	−55 to	+125 °C
Junction temperature	T_j	max.	150 °C

CHARACTERISTICS

T_{amb} = 25 °C; I_L = 15 mA, unless otherwise specified. See also Fig. 11.

description	symbol	min.	typ.	max.	unit
Supply					
Line voltage d.c.					
I_L = 15 mA	V_L	4,5	4,8	5,1	V
I_L = 50 mA	V_L	4,7	5,0	5,3	V
I_L = 100 mA	V_L	5,0	5,4	6,5	V
Temperature coefficient	TC	–	−8	–	mV/K
Line current range	I_L	10	–	120	mA
Stabilized voltage (pin 3)					
I_L = 15 mA	V_S	–	3,3	–	V
I_L = 100 mA	V_S	–	3,8	–	V
Reference voltage (pin 12)	V_R	–	1,0	–	V

description	symbol	min.	typ.	max.	unit
Microphone					
Input resistance (symmetrical)	R_i 13-14	–	4	–	kΩ
Input resistance (asymmetrical)	R_i 13	–	22	–	kΩ
Voltage amplification f = 800 Hz; R_L = 600 Ω	A_M	48	50	52	dB
Temperature coefficient I_L = 50 mA; T_{amb} = –5 to +45 °C	TC		t.b.f.		dB
Common mode rejection ratio	CMRR	60	–	–	dB
Distortion at V_L = 3 dBm	dt	–	2	–	%
Noise output voltage Z_L = 600 Ω; psophometrically weighted (P53 curve)	V_{NO}	–	–70	–	dBmp
Amplification reduction during dialling	ΔA_M	–	70	–	dB
Anti-sidetone					
Voltage amplification, microphone to anti-sidetone output (R_{AT} = 3,9 kΩ)	A_{AT}	–	25,8	–	dB
Transmitter output stage					
Dynamic resistance setting range	R_i	600	–	900	Ω
Variation over line current R_i = 600 Ω	ΔZ_o	–	100	–	Ω
Balance return loss from 300 up to 3400 Hz at 600 Ω (R_{ZI} = 75 Ω, C_L = 10 nF)	BRL	20	–	–	dB
at 900 Ω (R_{ZI} = 120 Ω, C_L = 30 nF)	BRL	20	–	–	dB
Telephone amplifier					
Voltage amplification R_T = 350 Ω	A_T	18	20	22	dB
Amplification variation f = 300 to 3400 Hz	$\Delta A_T/f$	–	0	–	dB
Amplification variation T = –5 to +45 °C	$\Delta A_T/T$	–	0	–	dB
Output voltage swing (d_t = 10%)	$V_{o(p-p)}$	–	1300	–	mV
Output impedance	Z_o	–	5	10	Ω
Input impedance	Z_i	–	100	–	kΩ
Output distortion level < –7 dBV	d_o	–	2	–	%
Output noise voltage psophometrically weighted (P53 curve)	$V_{no\ (rms)}$	–	–	500	μV
Bias current	I_M	3	3,5	4	mA

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

description	symbol	min.	typ.	max.	unit
DTMF generator					
Tone frequencies					
low tones (row inputs)			697, 770, 852, 941		Hz
high tones (column inputs)			1209, 1336, 1477, 1633		Hz
Dividing error					
crystal frequency = 4,78 MHz	Δf_d	−0,04	–	+0,11	%
crystal frequency = 3,58 MHz	Δf_d	−0,25	–	−0,05	%
Tone output level					
$I_L \geq 10$ mA					
lower tones	V_{LG}	–	−11	–	dBm
higher tones	V_{HG}	–	−9	–	dBm
Tone output level					
$I_L \geq 12$ mA					
lower tones	V_{LG}	−11	–	−6	dBm
higher tones	V_{HG}	−9	–	−4	dBm
Tolerance on output level					
over temp. and current range	ΔV_o	−2	–	2	dB
Pre-emphasis higher tones					
over temp. and current range	ΔV_{HG}	1,3	2	2,7	dB
Tone delay					
after key actuation	t_d	–	10	–	μs
Switch delay time speech/mute					
after key release	t_d	–	10	–	μs
Switch bounce elimination	t_{sb}	–	2	–	ms
Keyboard inputs					
Contact off resistance	R_{Koff}	250	–	–	kΩ
Contact on resistance	R_{Kon}	–	–	10	kΩ
Lower frequency inputs (ROW1, 2, 3, 4)					
voltage LOW	V_{IL}	–	0,7	t.b.f.	V
voltage HIGH	V_{IH}	t.b.f.	1,7	–	V
current (d.c.) at V_{IL}	I_{IL}	–	20	1000	μA
current (d.c.) at V_{IH}	I_{IH}	–	–	–	μA
Higher frequency inputs (COL1, 2, 3, 4)					
voltage LOW	V_{IL}	–	0,3	t.b.f.	V
voltage HIGH	V_{IH}	t.b.f.	1,0	–	V
current (d.c.) at V_{IL}	I_{IL}	–	–	–	μA
current (d.c.) at V_{IH}	I_{IH}	–	20	1000	μA

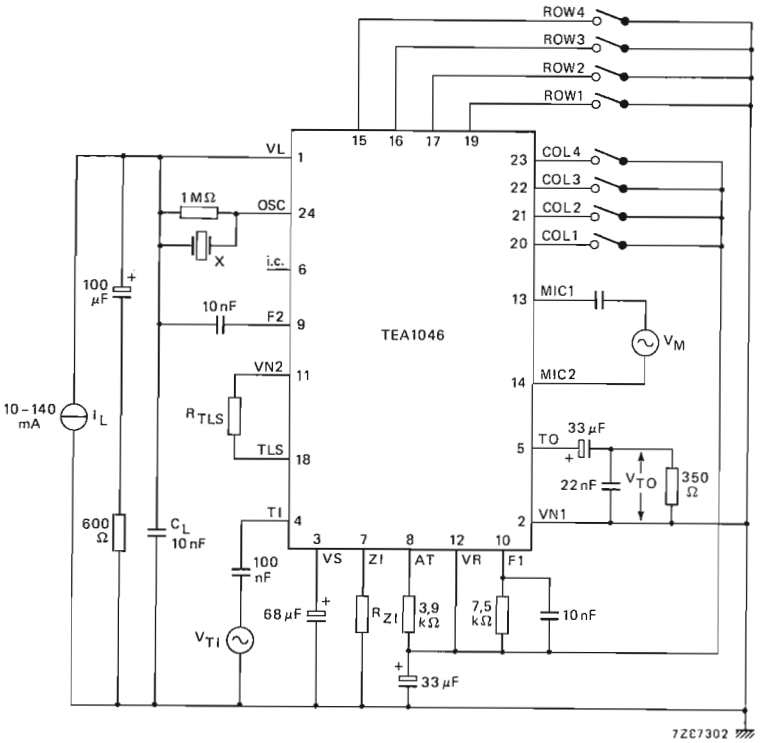


Fig. 11 Test circuit for measuring amplifier voltage gains and frequencies and levels of DTMF generator.
X = 3,58 or 4,78 MHz.

$$A_M = \left| \frac{V_L}{V_M} \right| \quad (V_{TI} = 0) \qquad A_T = \left| \frac{V_{TO}}{V_{TI}} \right| \quad (V_M = 0) \qquad A_{AT} = \left| \frac{V_{AT}}{V_M} \right| \quad (V_{TI} = 0)$$

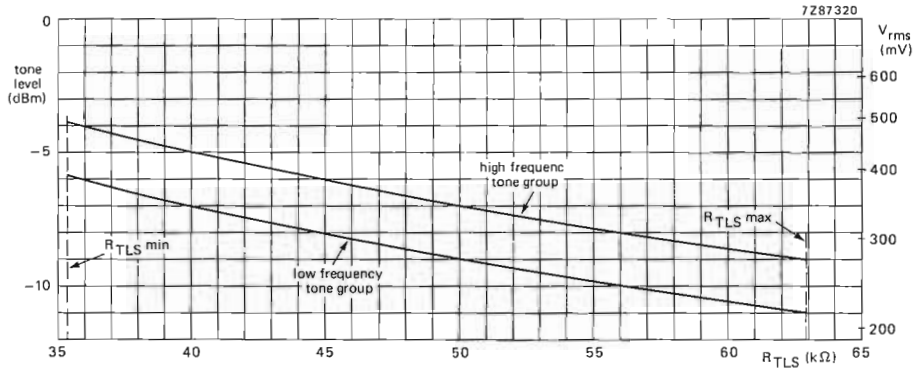


Fig. 12 DTMF level selection. The curve is valid for a dynamic impedance of 600 Ω (R_{ZI} = 75 Ω).

Some values:

LOW dBm	HIGH dBm	R_{TLS} kΩ
−6	−4	35,2
−8	−6	44,8
−11	−9	62,6

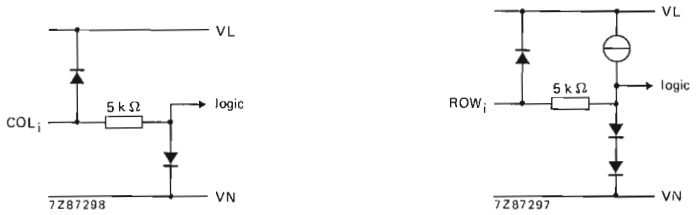


Fig. 13 Configuration inputs. (a) ROW1, 2, 3 and 4. (b) COL1, 2, 3 and 4.

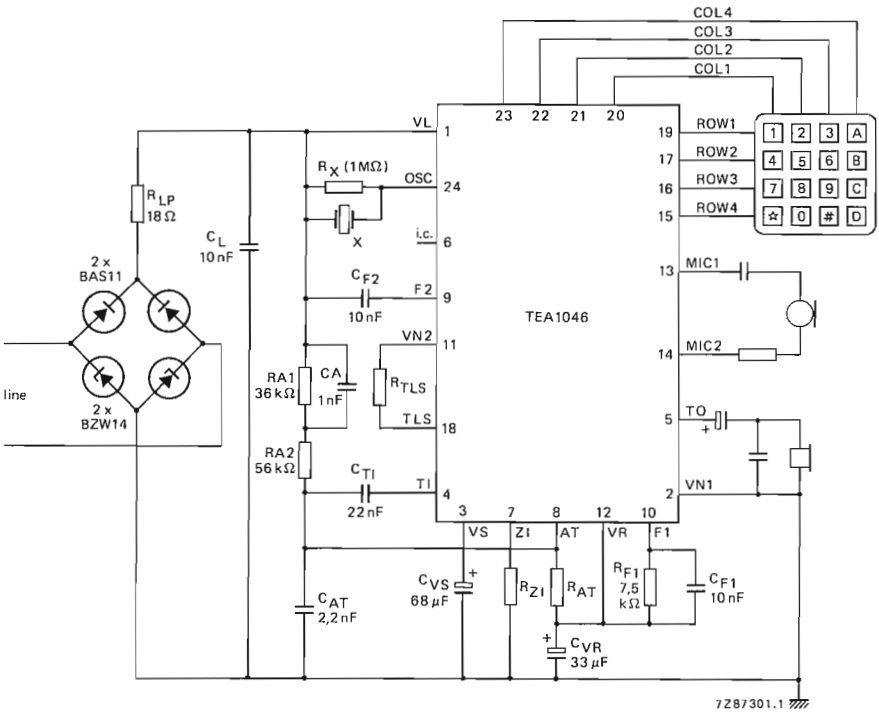
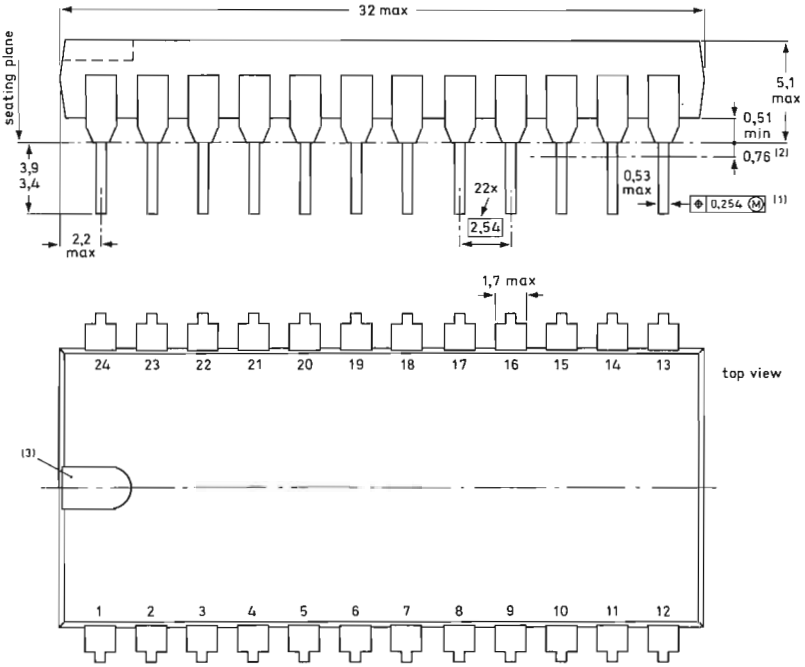
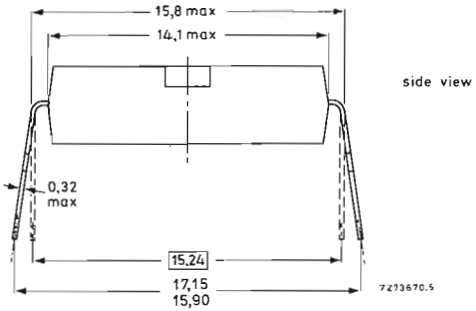


Fig. 14 Application diagram TEA1046 using dynamic transducers, R_{MS}, R_{AT}, R_{ZI} and R_{TLS} determined by transducers and system requirements.

DEVELOPMENT SAMPLE DATA

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See next page.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

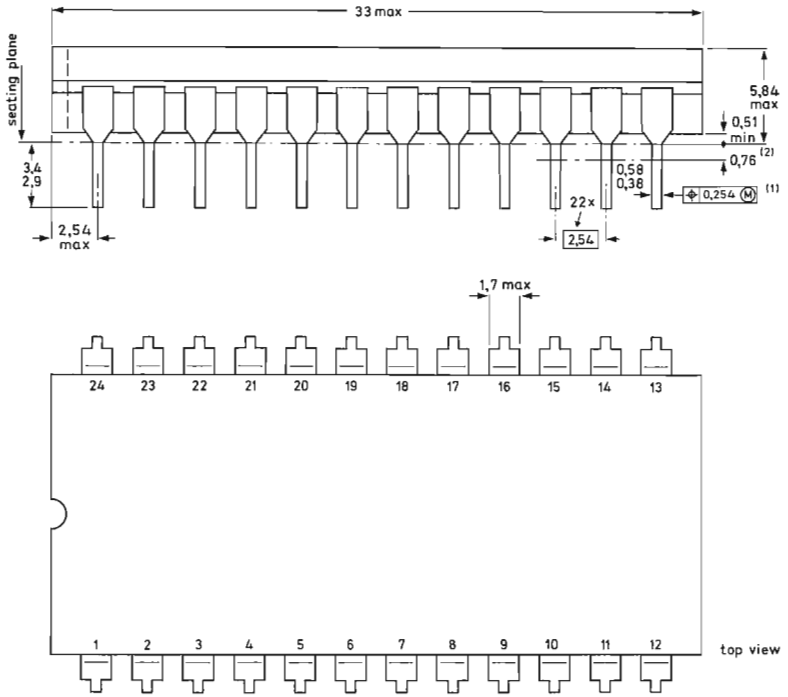
2. By dip or wave

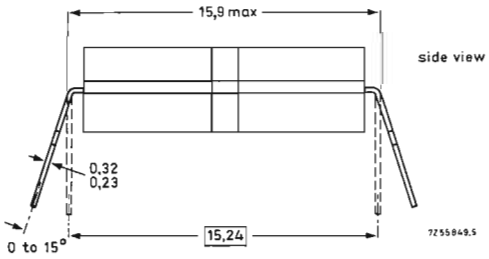
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

24-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-94)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

MICROPHONE AMPLIFIER

GENERAL DESCRIPTION

The TCA980G is a bipolar integrated microphone amplifier. It is primarily intended for use with low-impedance microphones in telephone systems. The output of the amplifier is 210 V/kPa when used with a microphone having an impedance of 200 Ω and a sensitivity of 10 mV/kPa.

A capsule assembly containing the TCA980G, a low-impedance microphone and a 220 nF capacitor can directly replace a carbon microphone. The circuit is intended to be supplied from the telephone line, the line current may be of either polarity.

QUICK REFERENCE DATA

Supply current range	$\pm I_{LN2}$	10 to 100	mA
Supply voltage drop at $\pm I_{LN2}$ = 10 mA	$\lvert V_{LN1}-V_{LN2}\rvert$	typ. 4,75	V
Voltage amplification at $\pm I_{LN2}$ = 30 mA	A_{vd}	typ. 220	
at $\pm I_{LN2}$ = 10 mA	A_{vd}	min. 160	
Output impedance at $\pm I_{LN2}$ = 30 mA	$\lvert z_{od}\rvert$	typ. 150	Ω
Operating ambient temperature range	T_{amb}	−35 to +75	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

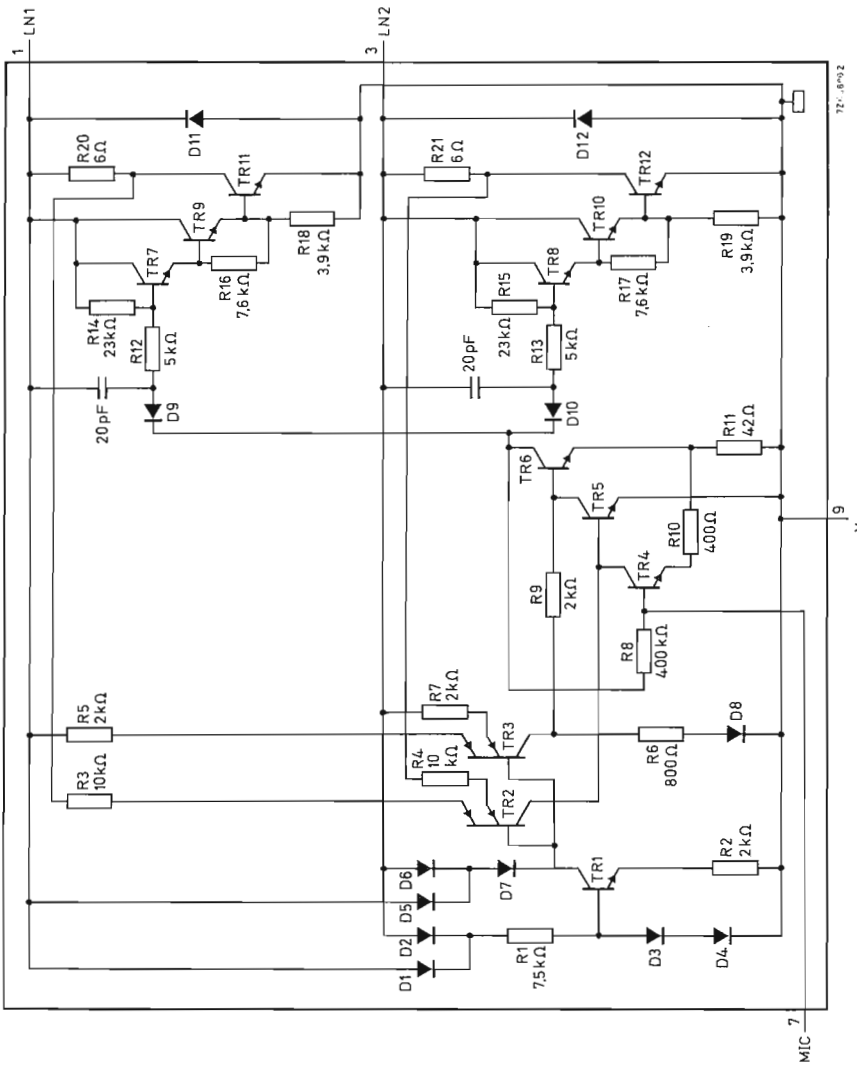


Fig. 1 Circuit diagram.

PHILIPS

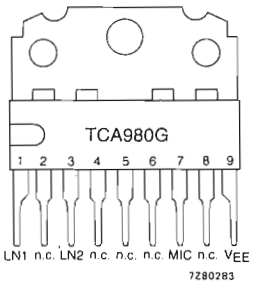


Fig. 2 Pinning diagram.

PINNING

1	LN1	line terminal 1
2	n.c.	not connected
3	LN2	line terminal 2
4	n.c.	not connected
5	n.c.	not connected
6	n.c.	not connected
7	MIC	microphone input
8	n.c.	not connected
9	V_{EE}	reference

FUNCTIONAL DESCRIPTION

At its line terminals LN1 and LN2 the TCA980G is compatible with a classical carbon microphone. The circuit then is supplied from the telephone line and produces its own supply voltage, irrespective of the direction of line current flow. The output voltage is produced across the same line terminals LN1 and LN2. The circuit is well stabilized with the result that circuit properties such as gain and d.c. voltage drop vary little with line current.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current, LN1 and LN2		
d.c.	$\pm I_{LN}$	max. 100 mA
non-repetitive peak	$\pm I_{LN(SM)}$	max. 100 mA a.c. superimposed on 100 mA d.c.
Input current, d.c.	$\pm I_{MIC}$	max. 100 μA
Total power dissipation	P_{tot}	see Fig. 3
Storage temperature range	T_{stg}	−55 to +125 °C
Operating ambient temperature range	T_{amb}	−35 to +75 °C

CHARACTERISTICS

$\pm I_{LN2}$ = 10 to 60 mA; T_{amb} = 25 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage drop					
at $\pm I_{LN2}$ = 10 mA	$\lvert V_{LN1} - V_{LN2}\rvert$	3,5	4,75	5,75	V
at $\pm I_{LN2}$ = 30 mA	$\lvert V_{LN1} - V_{LN2}\rvert$	4,45	–	6,75	V
at $\pm I_{LN2}$ = 60 mA	$\lvert V_{LN1} - V_{LN2}\rvert$	5,0	–	7,8	V
Gain					
Voltage amplification at f = 2 kHz; T_{amb} = 25 °C; see Fig. 4;					
at $\pm I_{LN2}$ = 10 mA	A_{vd}	160	–	260	
at $\pm I_{LN2}$ = 30 mA	A_{vd}	190	220	260	
Variation of voltage amplification with temperature for T_{amb} = –20 to +55 °C	$\Delta A_{vd}/A_{vd}$	–	–	10	%
Variation of voltage amplification with frequency for f = 0,3 to 2 kHz	ΔA_{vd}	–	1	3	dB
Output					
Output voltage swing, clipped,					
at $\pm I_{LN2}$ = 10 mA	$V_{LN1\text{-}LN2(p\text{-}p)}$	2,6	–	–	V
at $\pm I_{LN2}$ = 30 mA	$V_{LN1\text{-}LN2(p\text{-}p)}$	3,5	–	–	V
at $\pm I_{LN2}$ = 60 mA	$V_{LN1\text{-}LN2(p\text{-}p)}$	2,6	–	–	V
A.C. output voltage at f = 2 kHz; d_{tot} = 5%;					
at $\pm I_{LN2}$ = 10 mA	$V_{LN1\text{-}LN2(rms)}$	1	–	–	V
at $\pm I_{LN2}$ = 30 mA	$V_{LN1\text{-}LN2(rms)}$	1,35	–	–	V
at $\pm I_{LN2}$ = 60 mA	$V_{LN1\text{-}LN2(rms)}$	–	1,5	–	V
Noise output voltage at B = 0,3 to 4 kHz	$V_{n(rms)}$	–	–	1,3	mV
Output impedance at f = 2 kHz; $\pm I_{LN2}$ = 30 mA	$\lvert z_{od}\rvert$	–	150	–	Ω

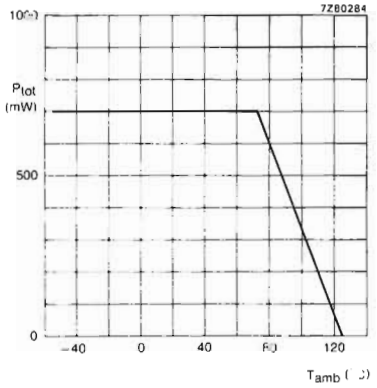


Fig. 3 Power derating curve.

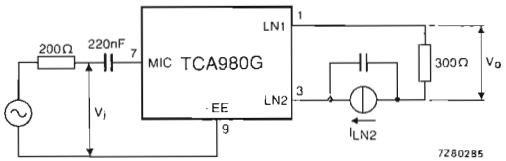


Fig. 4 Test circuit for voltage gain.

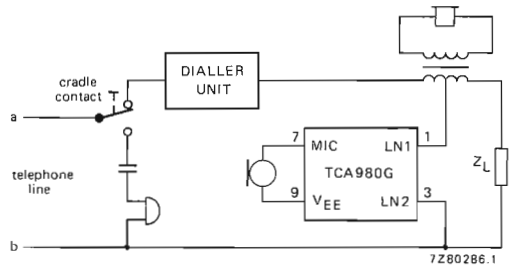
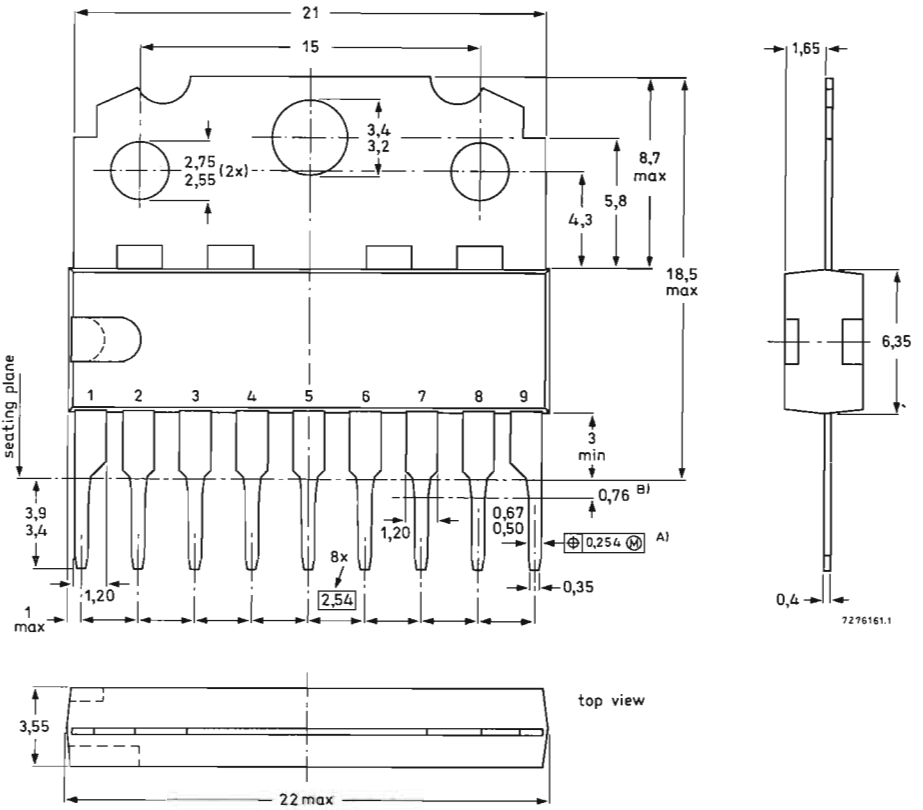


Fig. 5 Typical application of the TCA980G. At pins LN1 and LN2, the IC is compatible with a carbon microphone in a classical subscriber set.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110B)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

AUDIO AMPLIFIER

The TBA915G is a bipolar integrated a.f. amplifier intended for small communication receivers, where low battery drain is of paramount importance. The maximum output power is 850 mW and the zero-signal supply current is only 2 mA (typ.). The circuit can be squelched to a stand-by current of typ. 0,4 mA.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		3,5 to 15 V
Supply current at V_{CC} = 12 V			
squelched	I_{CC}	typ.	0,4 mA
no signal	I_{CC}	typ.	2 mA
P_o = 500 mW	I_{CC}	typ.	72 mA
Input signal for P_o = 500 mW	$V_{i(rms)}$	typ.	10 mV
Input impedance, single-ended	$\lvert z_{is} \rvert$	typ.	9 kΩ
Output power at d_{tot} = 2,5%	P_o	typ.	500 mW
Operating ambient temperature range	T_{amb}		−20 to +80 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

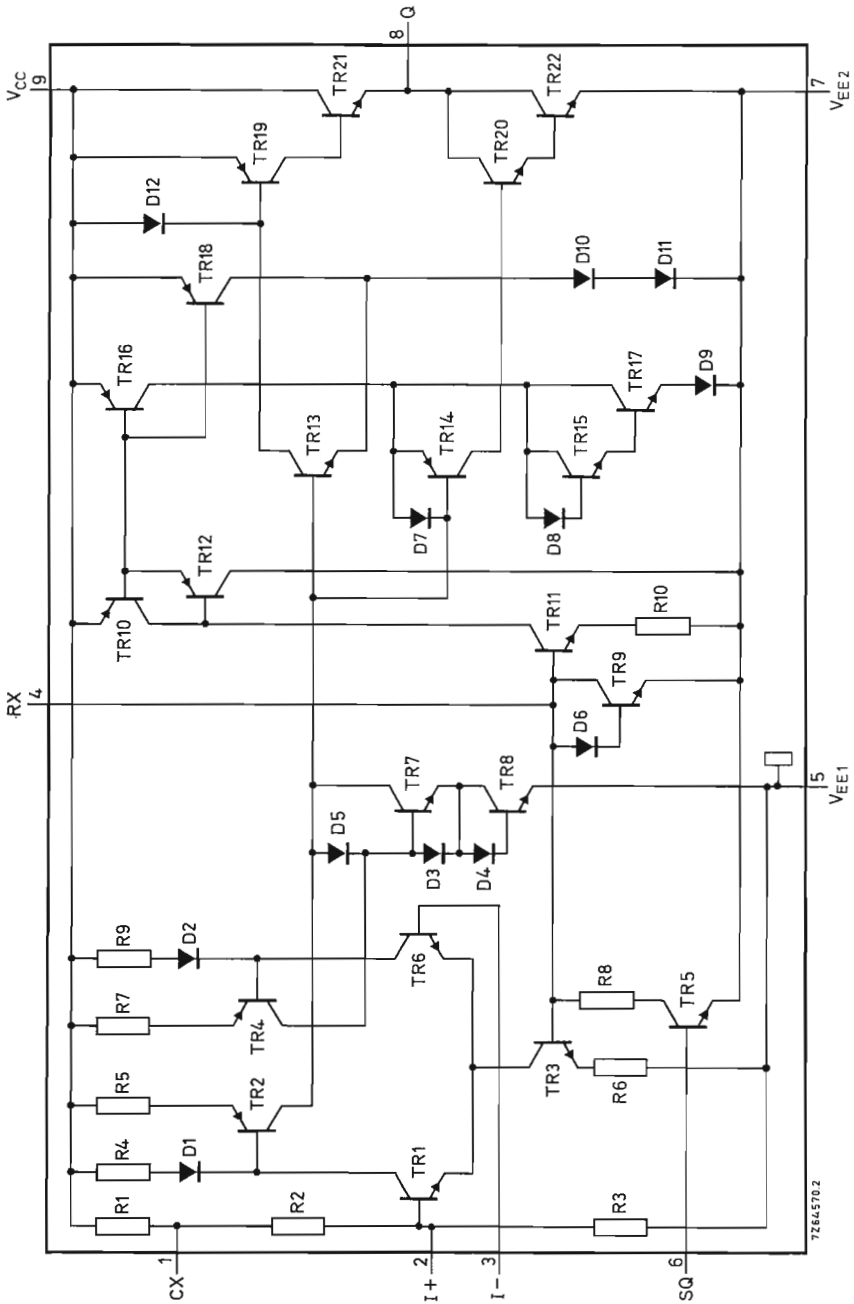


Fig. 1 Circuit diagram.

PHILIPS

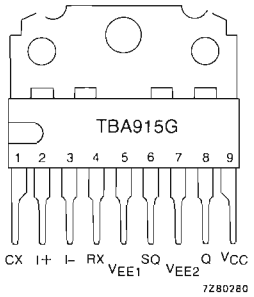


Fig. 2 Pinning diagram.

PINNING

1	CX	external capacitor
2	I+	non-inverting input
3	I−	inverting input
4	RX	external resistor
5	V_{EE1}	ground
6	SQ	squelch input
7	V_{EE2}	ground
8	Q	output
9	V_{CC}	positive supply

FUNCTIONAL DESCRIPTION

Supply V_{CC} and RX (pins 9 and 4)

The TBA915G has been designed primarily for use in pocket-size portable communication receivers, with a low supply current as its main feature. The supply current is mainly determined by the output current. The current into the RX connection sets an internal current source.

The circuit may be used over a wide range of supply voltages, viz. 3,5 to 15 V. At 12 V the circuit is capable of delivering a power of 500 mW into a load of 20 Ω. The maximum output power may be increased to 850 mW by increasing the supply voltage to 14 V and reducing the load impedance to 15 Ω.

Inputs I+ and I− (pins 2 and 3)

Inputs I+ and I− are differential inputs. I+ is the non-inverting input, I− the inverting input. The circuit may be driven asymmetrically, as is done in the test circuit of Fig. 4, where I− is used as a feedback input. The circuit has an open-loop gain of 60 dB.

Squelch input SQ (pin 6)

A current into the SQ input squelches the amplifier, it brings the circuit in a stand-by state with a substantially reduced supply current.

Output Q (pin 8)

The circuit has a quasi-complementary class-B output stage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	17	V
Supply current	I_{CC}	max.	350	mA
Bias current into RX	I_{RX}	max.	5	mA
Input voltage, differential, I + and I− inputs	$\|V_{ID}\|$	max.	5	V
Input current, I + and I− inputs	I_I	max.	0,5	mA
Input current, SQ input	I_{SQ}	max.	1	mA
	$-I_{SQ}$	max.	10	μA
Output voltage	V_Q	max.	17	V
Output current	$\pm I_Q$	max.	350	mA
Total power dissipation	P_{tot}	max.	900	mW
Storage temperature range	T_{stg}	−55 to	+125	°C
Operating ambient temperature range	T_{amb}	−20 to	+80	°C

CHARACTERISTICS

V_{CC} = 12 V; V_{EE} = 0 V; T_{amb} = 25 °C; measured in test circuit Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC}					
Supply current					
squelched	I_{CC}	–	0,4	0,6	mA
quiescent	I_{CC}	–	2	3,7	mA
P_o = 500 mW	I_{CC}	–	72	–	mA
Variation of quiescent supply current with supply voltage	$\Delta I_{CC}/\Delta V_{CC}$	–	0,06	–	mA/V
Thermal resistance	$R_{th\ j\text{-}a}$	–	50	–	K/W
RX					
Bias current into RX	I_{RX}	25	–	75	μA
Inputs I + and I−					
Input voltage for P_o = 500 mW	$V_{i(rms)}$	–	10	15	mV
Input impedance, single-ended	$\|z_{is}\|$	–	9	–	kΩ
Open-loop differential voltage amplification	A_{vd}	–	60	–	dB
Squelch input SQ					
Input current HIGH (circuit squelched) at I_{RX} = 25 to 75 μA	I_{SQH}	10	–	–	μA
Input voltage HIGH at I_{SQH} = 10 μA	V_{SQH}	–	0,65	–	V
Input voltage LOW (circuit on)	V_{SQL}	–	–	0,4	V
Output Q					
Total distortion at P_o = 500 mW	d_{tot}	–	2,5	5	%
Signal-to-noise ratio at P_o = 500 mW; R_S = 600 Ω, f = 300 Hz to 6 kHz	S/N	–	72	–	dB

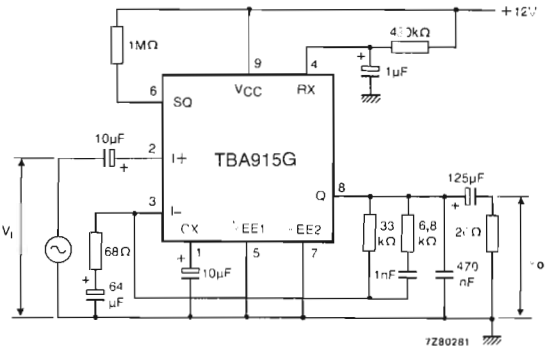


Fig. 3 Test circuit.

APPLICATION INFORMATION

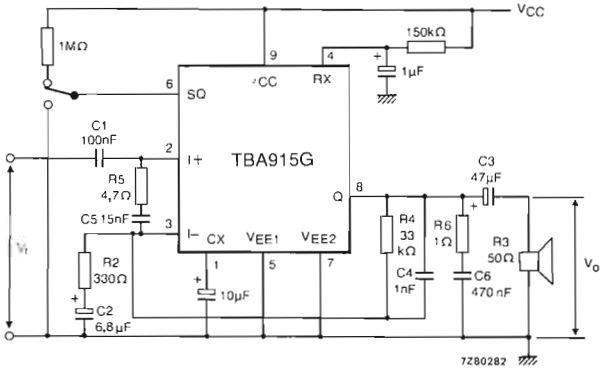


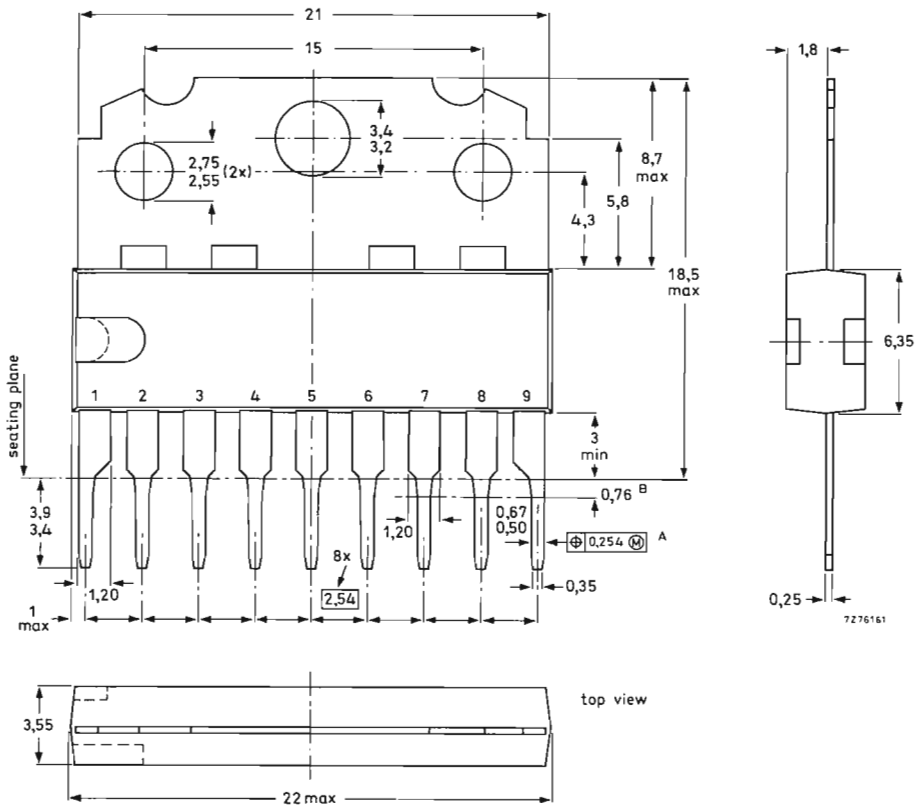
Fig. 4 Typical application of the TBA915G. The frequency range is 185 Hz to 5,2 kHz; the lower frequency limit is determined by the time constants $|z_{is}|$ x C1, R2 x C2 and R3 x C3 and the upper frequency limit by R4 x C4. The closed-loop gain is 39,5 dB with a stability margin greater than 18 dB which is determined by R5 x C5 and R6 x C6. The arrangement produces an output voltage and output power at 1 kHz which are (typical):

$V_{o(rms)}$ = 1,24 V, P_o = 30 mW at V_{CC} = 5 V and d_{tot} = 5%

$V_{o(rms)}$ = 1,7 V, P_o = 56 mW at V_{CC} = 6,8 V and d_{tot} = 0,25%

$V_{o(rms)}$ = 1,9 V, P_o = 72 mW at V_{CC} = 6,8 V and d_{tot} = 5%

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

CMOS ICs FOR TELEPHONE SUBSCRIBER SETS

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3320 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- All inputs with pull-up/pull-down (except CE).
- 23-digit capacity for redial operation.
- Circuit reset for line power breaks; > 160 ms.
- Dialling pulse frequency: 10 Hz.
- Test pulse frequency: 932 Hz.
- Hold facility for lengthening the inter-digit period.
- Memory overflow possibility (with internally disabled redial).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3320P: 18-lead DIL; plastic (SOT-102G).
PCD3320D: 18-lead DIL; ceramic (SOT-133).

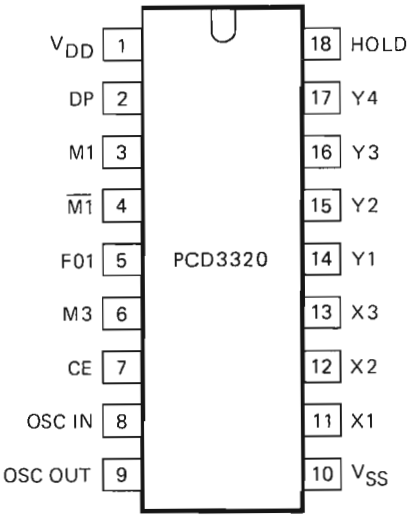


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

5	F01	the dialling pulse frequency is defined by the logic state of this input
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks.
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	
18	HOLD	interrupts dialling after completion of the current digit or immediately following an inter-digit pause (t_{id}); further keyboard data will be accepted

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	$\overline{M1}$	Muting; normally used for muting during the dialling sequence
4	$\overline{M1}$	inverted output of M1
6	M3	AND function, with $\overline{DP}$ and M1 as input, for direct drive of a switching transistor for dialling pulses and muting.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

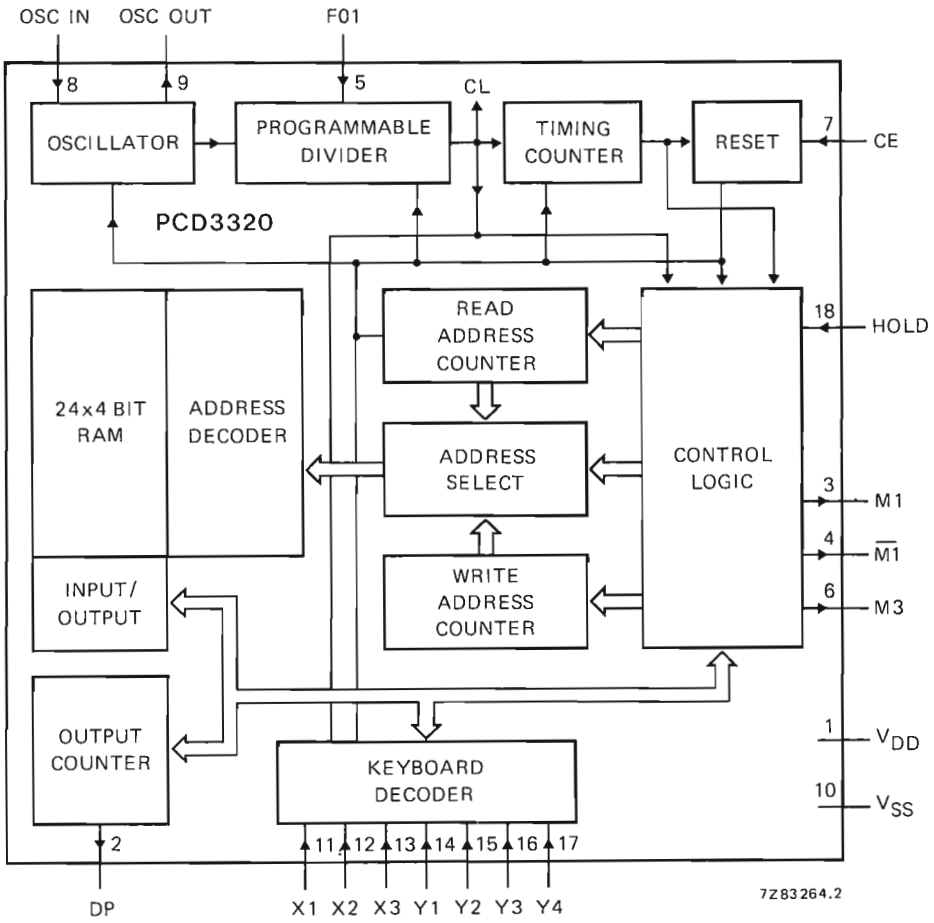


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3320 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set by input F01 to provide one of two chip system clocks; the 'normal' clock frequency (F01 = LOW) and the test frequency (F01 = HIGH).

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

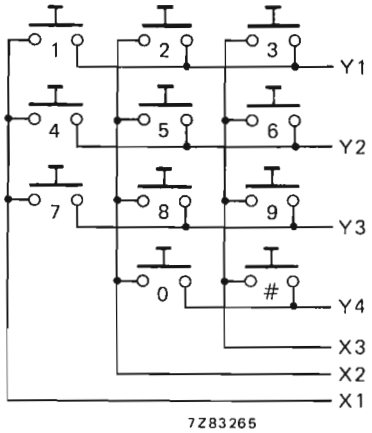
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored in the RAM and converted into correctly timed dialling pulses.



Redial.

Fig. 3 Single contact keyboard.

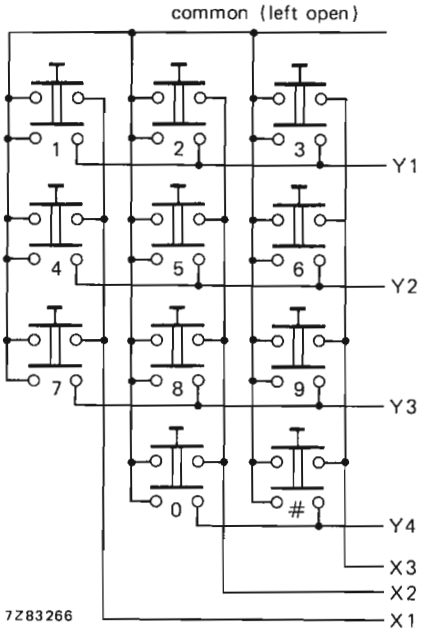


Fig. 4 Double contact keyboard.

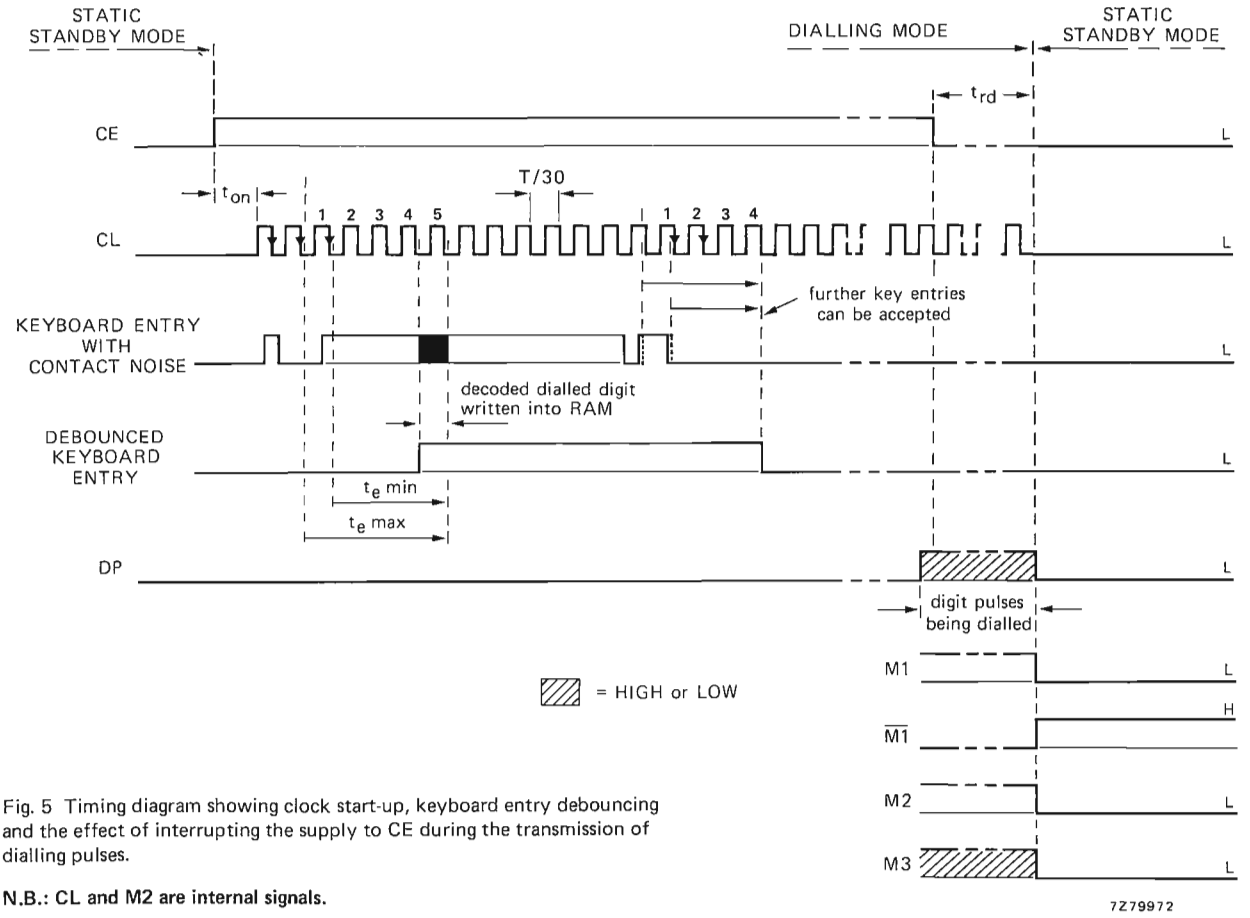


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

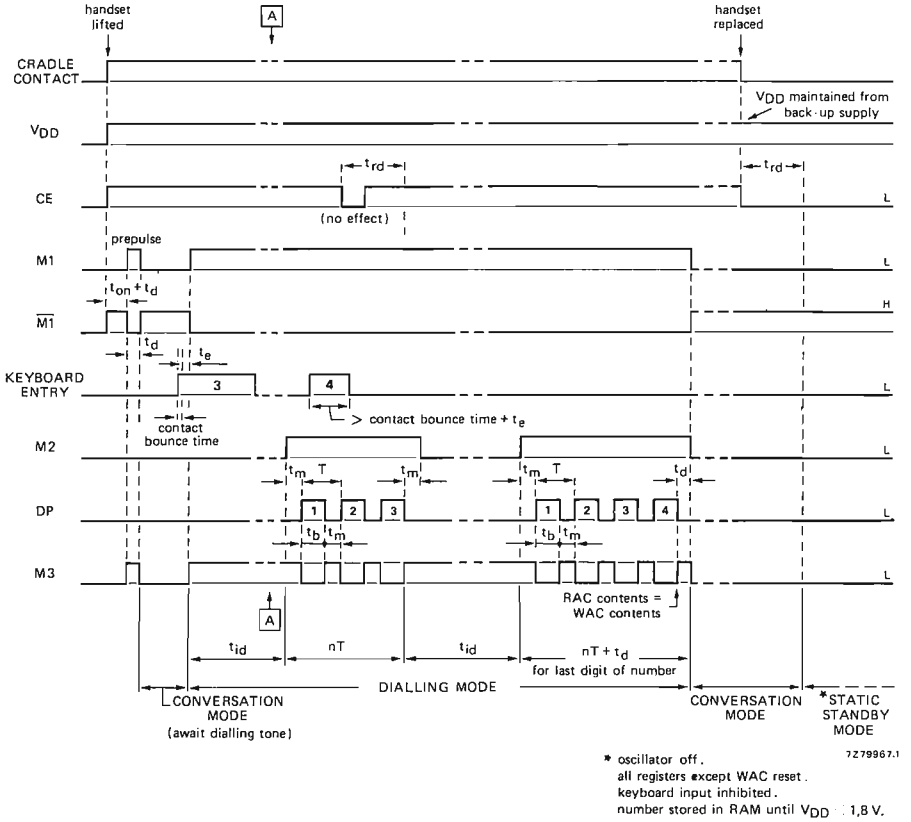


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

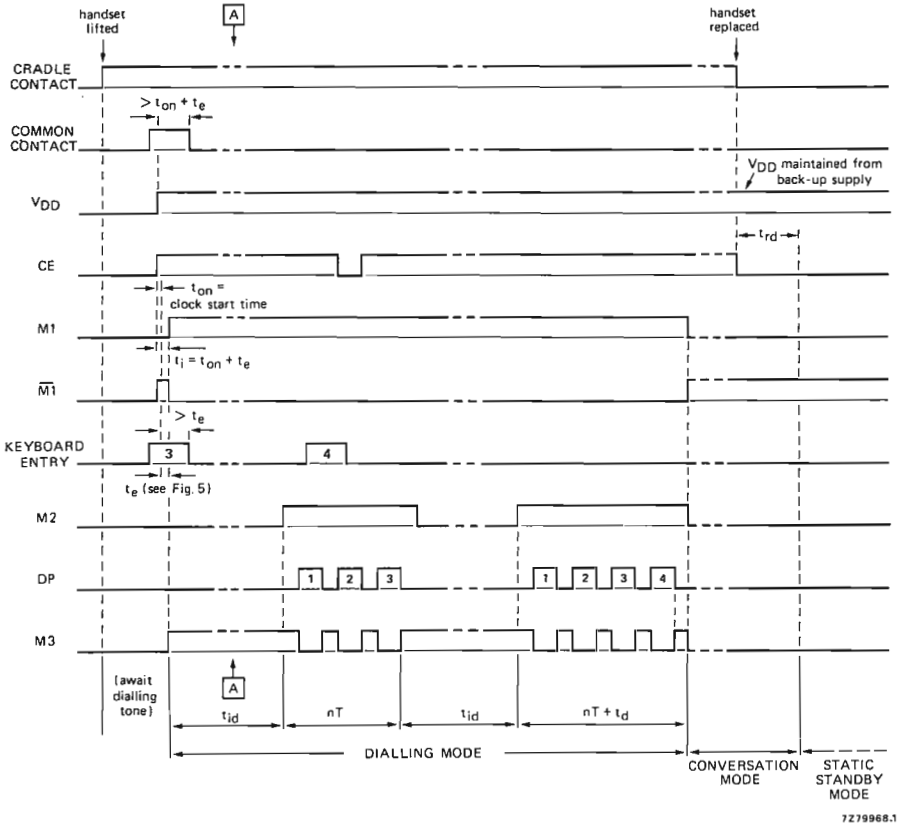


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

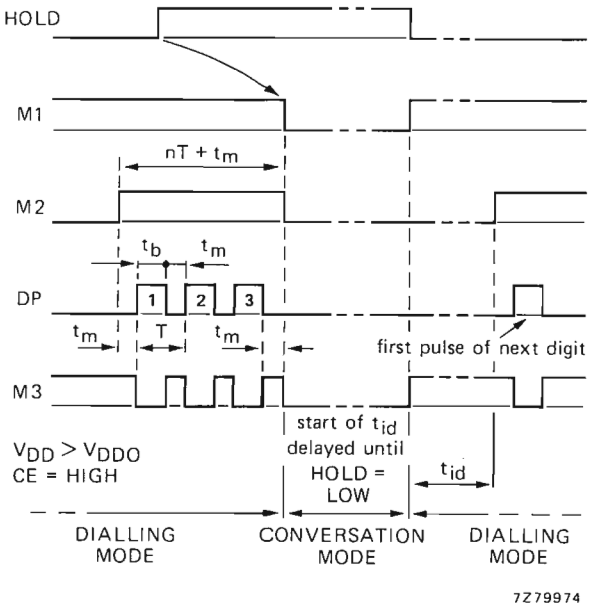


Fig. 8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses. M2 is an internal signal.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to + 70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to + 70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to + 70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ≤ V_{DD} ≤ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ≤ V_{DD} ≤ 6 V
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-down input current F01, HOLD	I_{IH}	30	100	300	nA	$V_I = V_{DD}$
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	$V_I = V_{SS}$
Output sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
Output source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

TIMING DATA I

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz; R_{Smax} = 100 Ω

	symbol	min.	typ.	max.		conditions
Clock start-up time	t_{on}	–	4	–	ms	Figs 6, 7; note 1
Initial data entry time ($t_i = t_{on} + t_e$)	$t_{i\,min}$	–	18	–	ms	F01 = LOW } Fig. 7
	$t_{i\,max}$	–	4	–	ms	F01 = HIGH }

TIMING DATA II (exact values)

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

	symbol	F01 = LOW (dialling)	F01 = HIGH (testing)		conditions
Dialling pulse frequency	f_{DP}	10,13	932,2	Hz	note 2
Dialling pulse period; $1/f_{DP}$	T_{DP}	98,7	1,073	ms	Figs 6, 7
Prepulse duration; 1/3 x T_{DP}	t_d	33	0,358	ms	Figs 6, 7
Inter-digit pause; 8 x T_{DP}	t_{id}	790	8,58	ms	Figs 6, 7
Break time; 3/5 x T_{DP}	t_b	59,2	0,644	ms	Fig. 6
Make time; 2/5 x T_{DP}	t_m	39,5	0,429	ms	Fig. 6
Debounce time					
min. 4/30 x T_{DP}	$t_{e\,min}$	13,2	0,143	ms	Fig. 5
max.; 1/6 x T_{DP}	$t_{e\,max}$	16,5	0,179	ms	Fig. 5
Reset delay time; 1,6 x T_{DP}	t_{rd}	158	1,7	ms	Figs 5, 6, 7

Notes

1. Stray capacitance between pins 8 and 9 < 3 pF.
2. Exactly 10 Hz and 920 Hz respectively when a 3,5328 MHz crystal is used.

TYPICAL CURVES

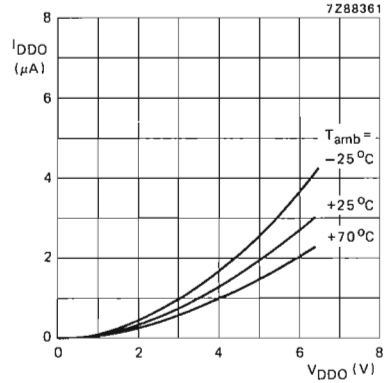


Fig. 9 Standby supply current as a function of standby supply voltage.

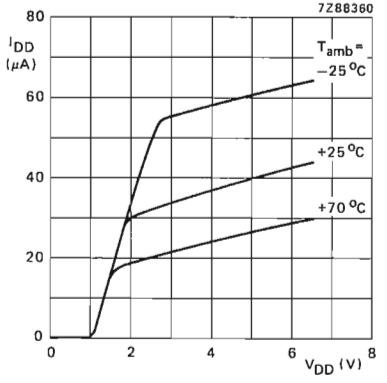


Fig. 10 Operating supply current as a function of operating supply voltage.

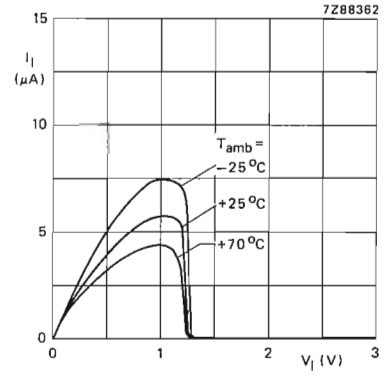


Fig. 11 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

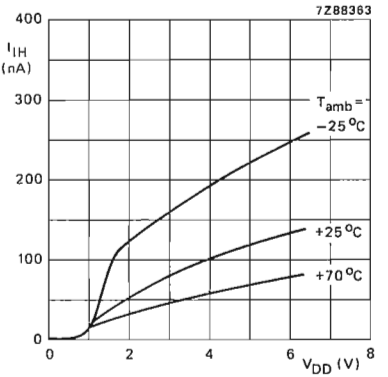


Fig. 12 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

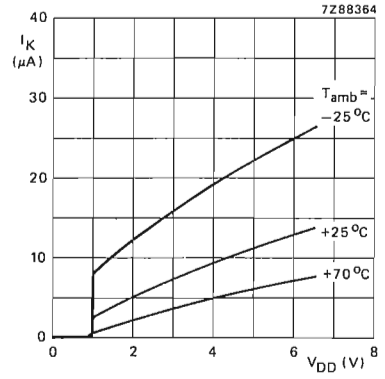


Fig. 13 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

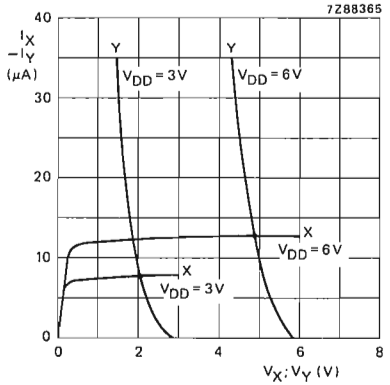


Fig. 14 Keyboard input characteristics at T_{amb} = 25 °C.

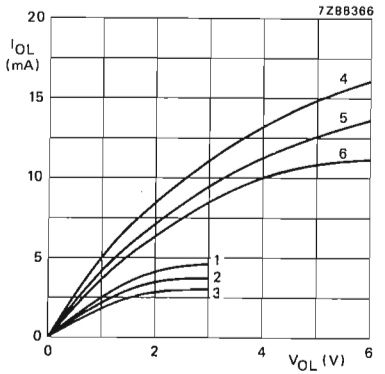


Fig. 15 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M3 and DP.

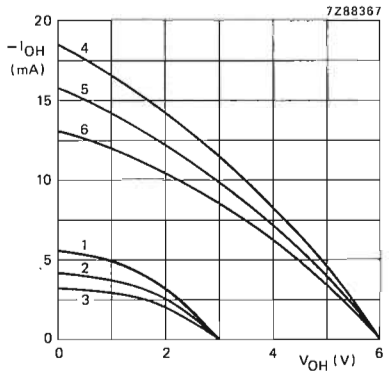
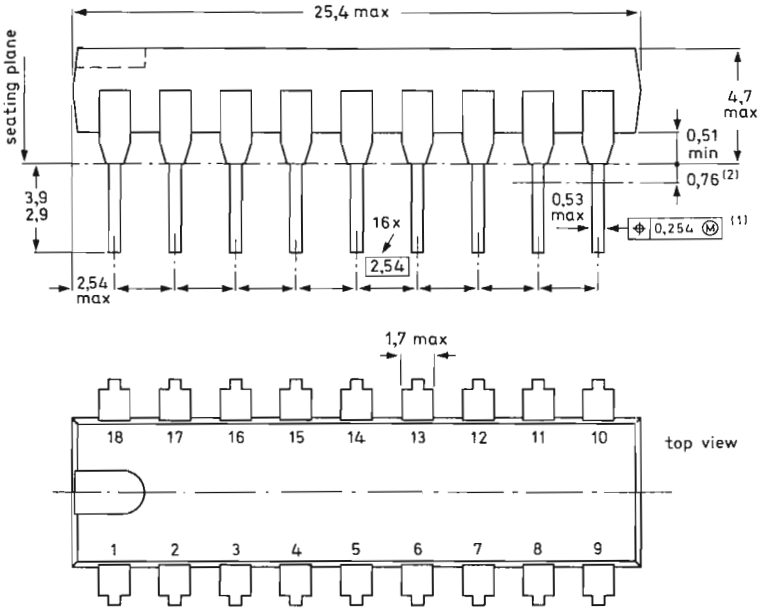


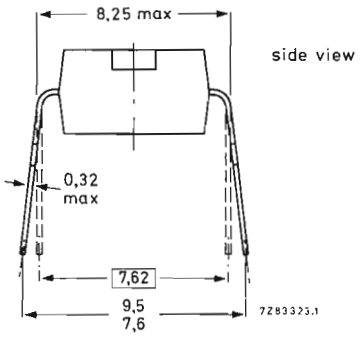
Fig. 16 Output (P-channel) source characteristics for M1, $\overline{M1}$, M3 and DP.

Curves for Figs 15 and 16

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102G)





⊕ Positional accuracy.

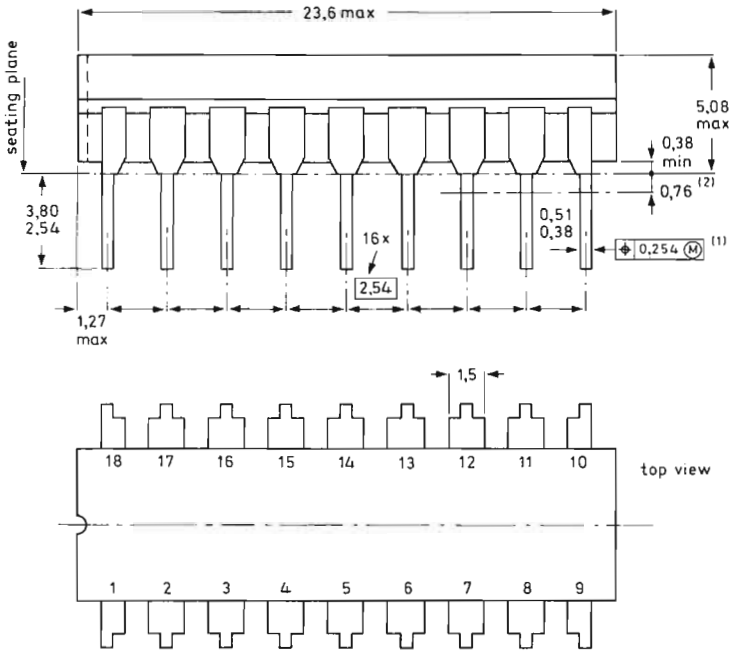
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

18-LEAD DUAL IN-LINE; CERAMIC (SOT-133)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3321 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3321 can regenerate access pauses during redial. During the original entry, access pauses are stored either automatically or via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems. The PCD3321 is pin to pin compatible with the DF320 and the MT4320 (however, including additional functions).

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; $>$ 160 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3321P: 18-lead DIL; plastic (SOT-102G).
PCD3321D: 18-lead DIL; ceramic (SOT-133).

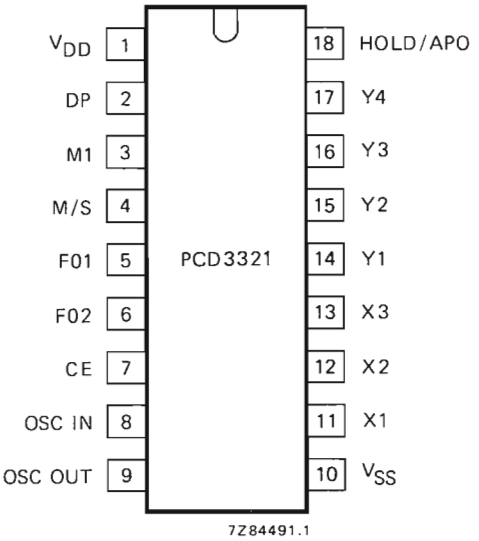


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

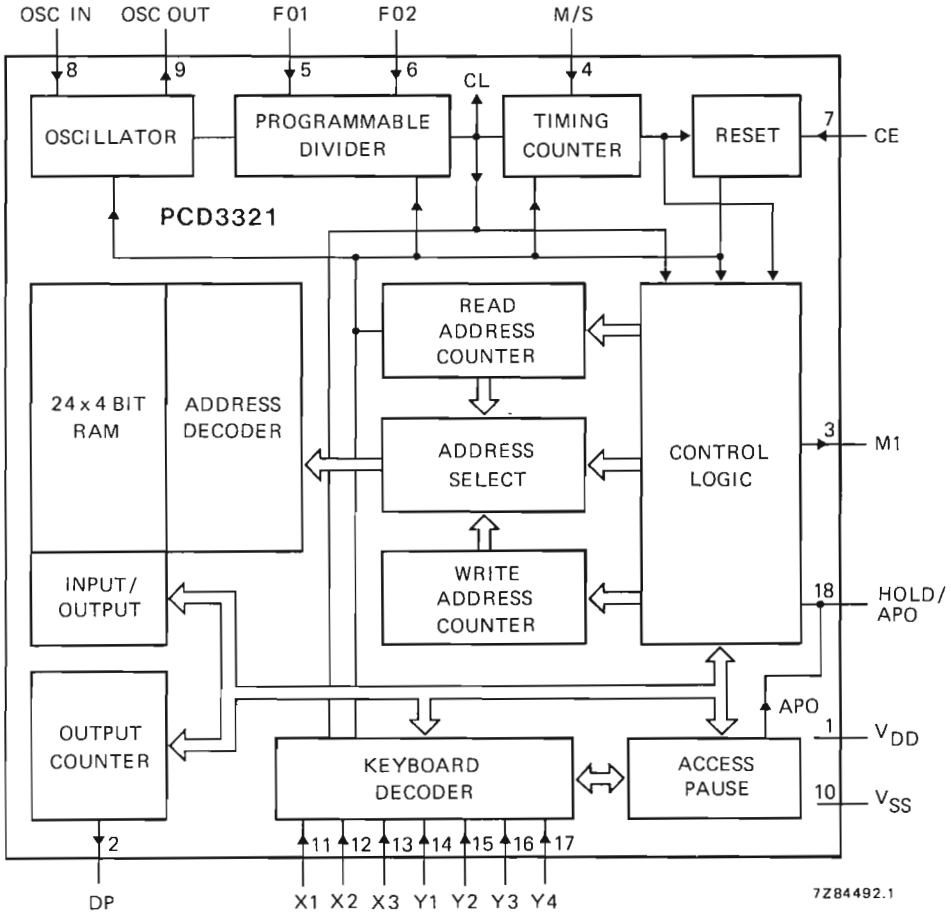


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3321 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

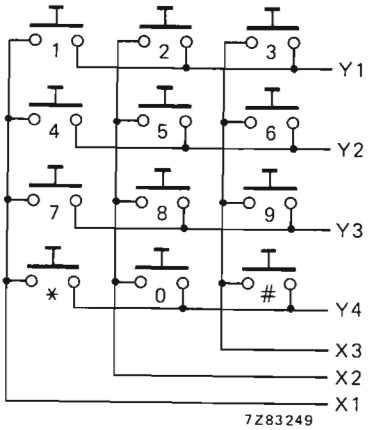
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3321. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

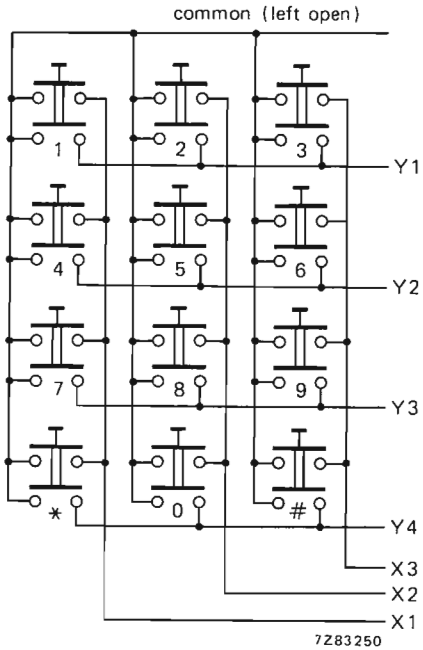


Fig. 4 Double contact keyboard.

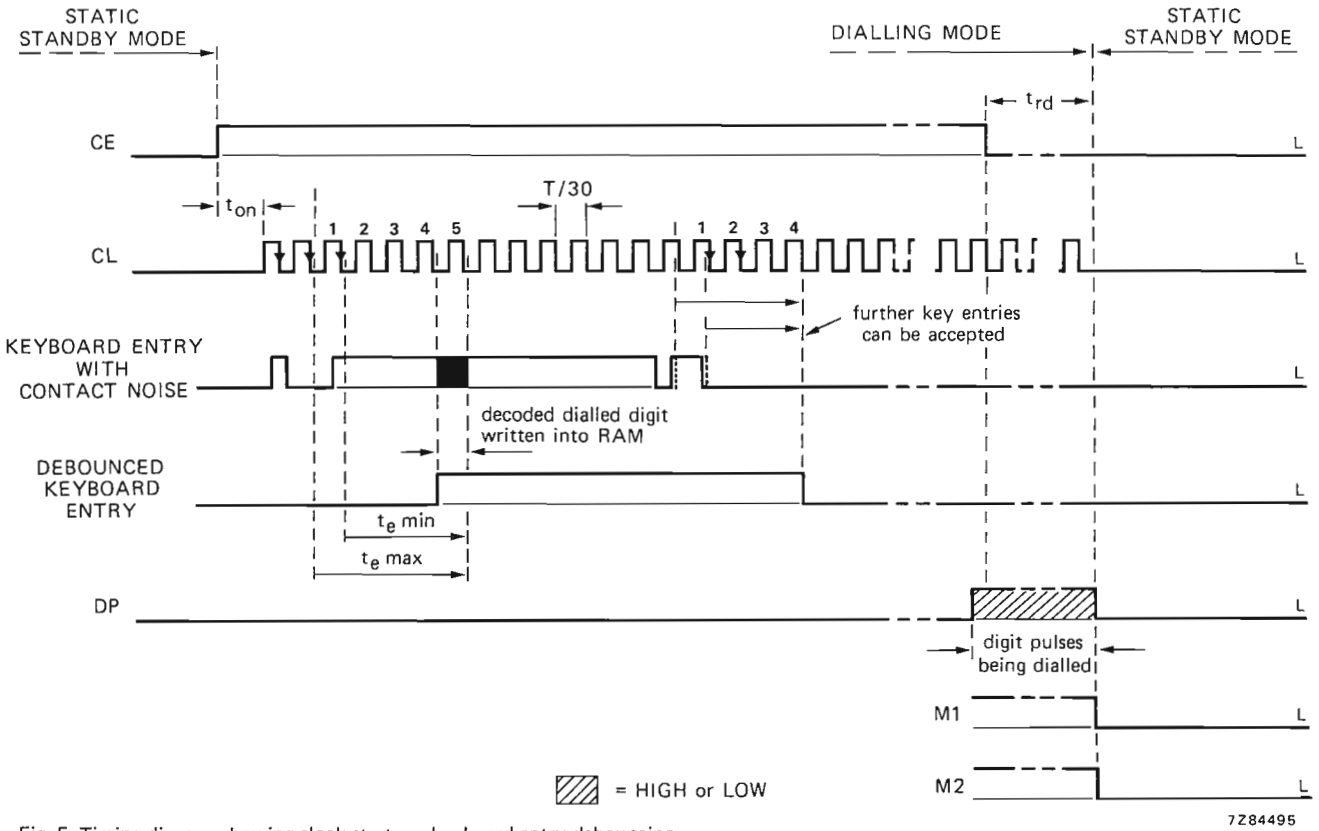


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

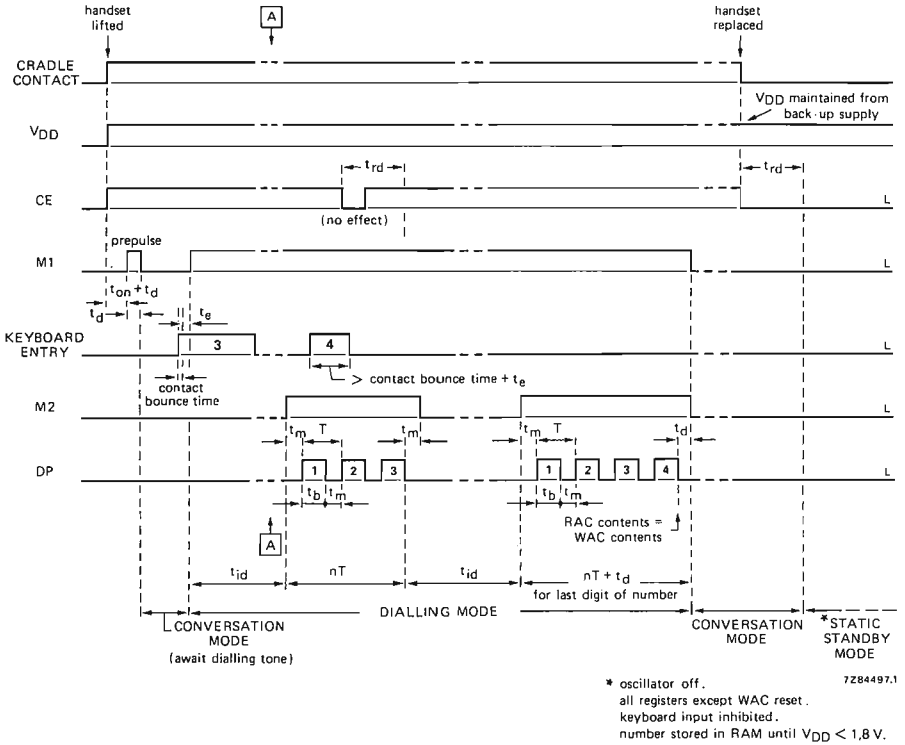


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

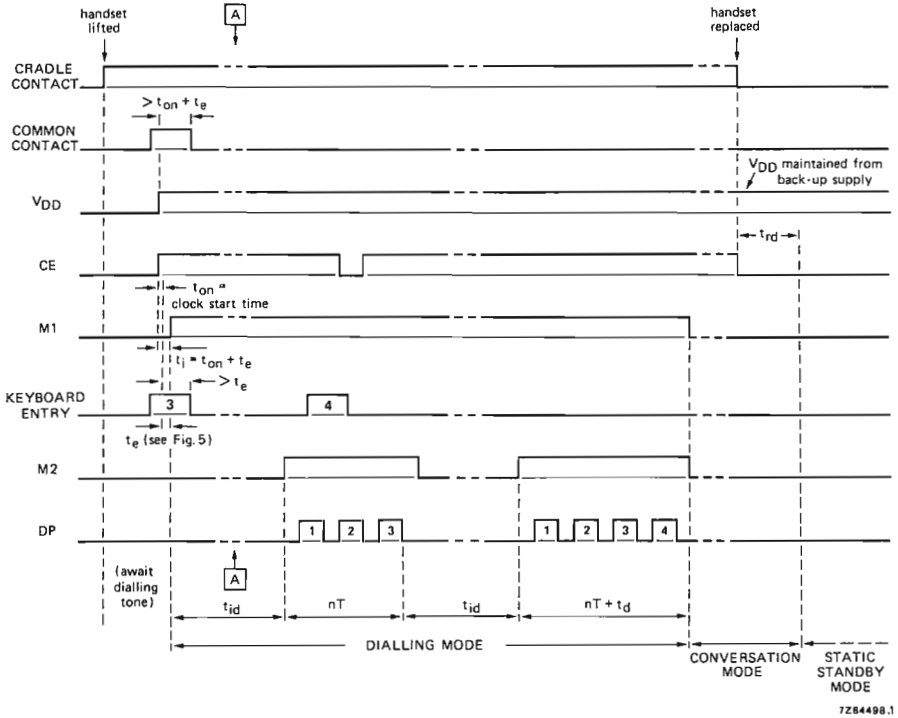


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

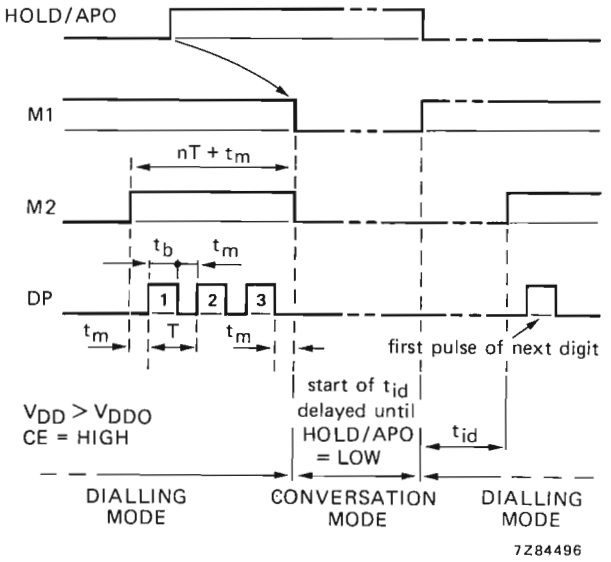


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

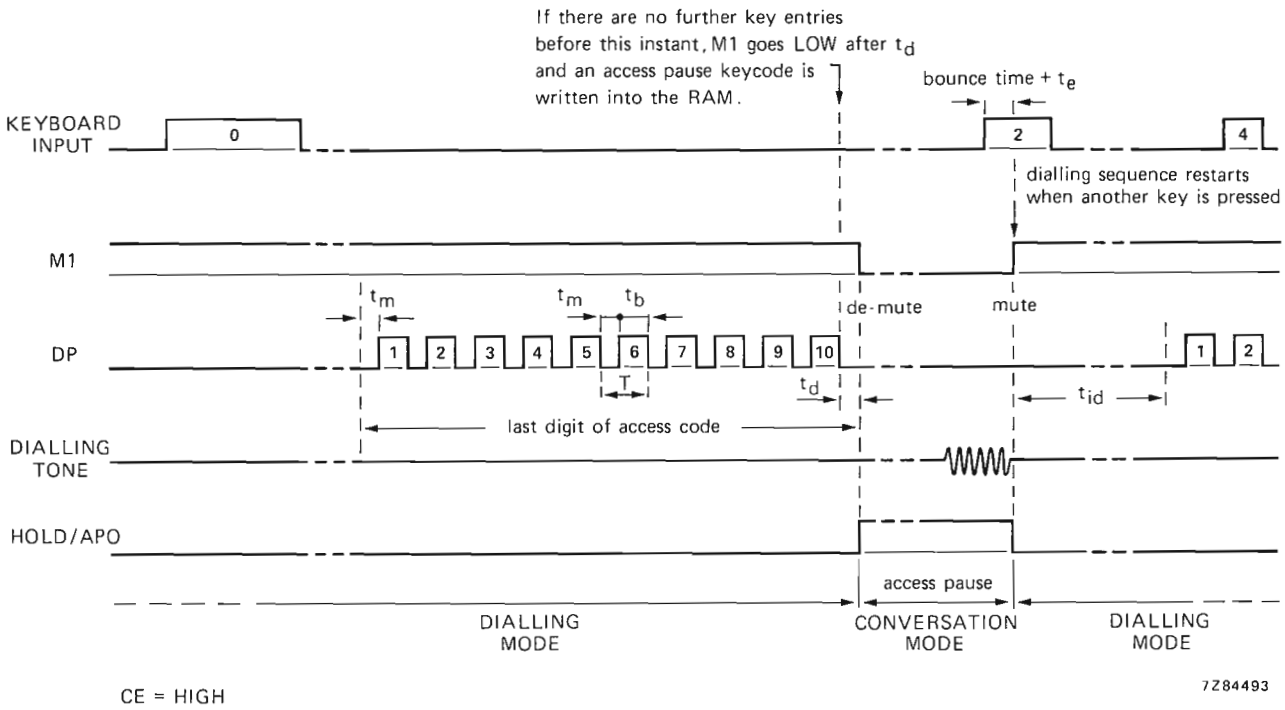
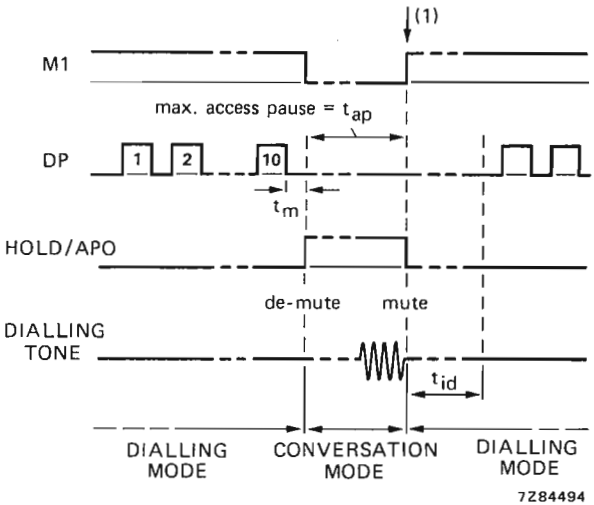


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO)will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Up to two access pauses can be entered into the RAM in this manner. Alternatively, the access pause key (★) can still be pressed to insert (more) access pauses manually (digits + access pauses ⩽ 23).
During redial, access pauses will be automatically regenerated.

Three methods of terminating an access pause:
1. Automatically, if the built-in time t_{ap} expires; HOLD/APO then goes LOW.
2. Manually, by pressing the redial key before t_{ap} expires.
3. With an external tone recogniser, by forcing HOLD/APO to LOW or HIGH respectively, for shortening or lengthening an access pause.



(1) a. Access pause (t_{ap}) expires or press redial before end of t_{ap}.

b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW before t_{ap} expires; access pause $< t_{ap}$
HOLD/APO forced to HIGH after t_{ap} expires; access pause $> t_{ap}$.

Fig. 10 Timing diagram showing Access Pause Reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 4)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	—	—	—	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 5)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. Mark-to-space ratio: 2:1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
5. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

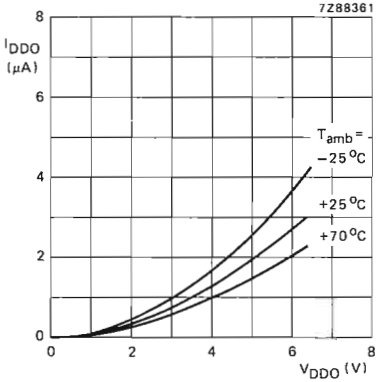


Fig. 11 Standby supply current as a function of standby supply voltage.

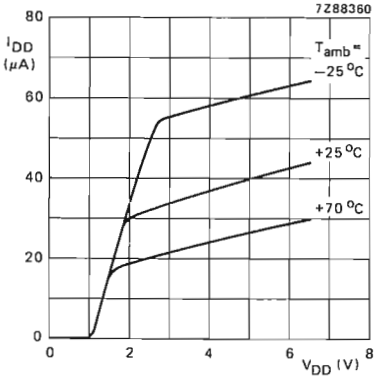


Fig. 12 Operating supply current as a function of operating supply voltage.

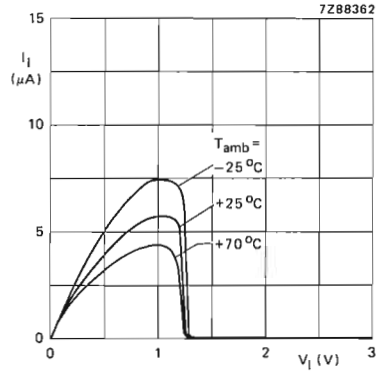


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

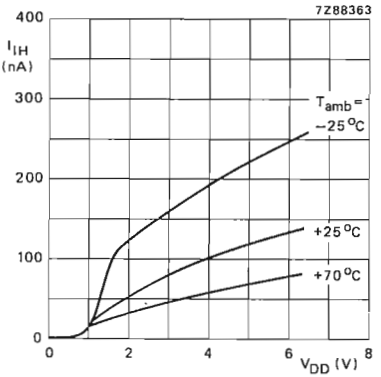


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

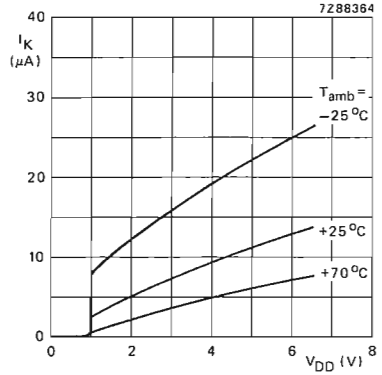


Fig. 15 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

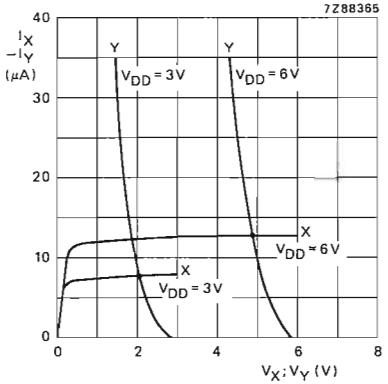


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

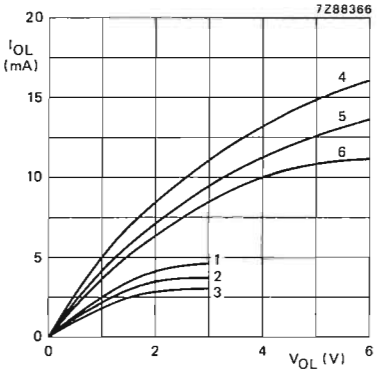


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

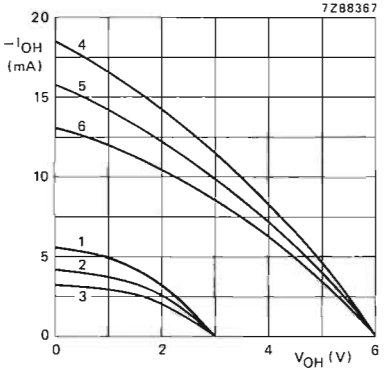
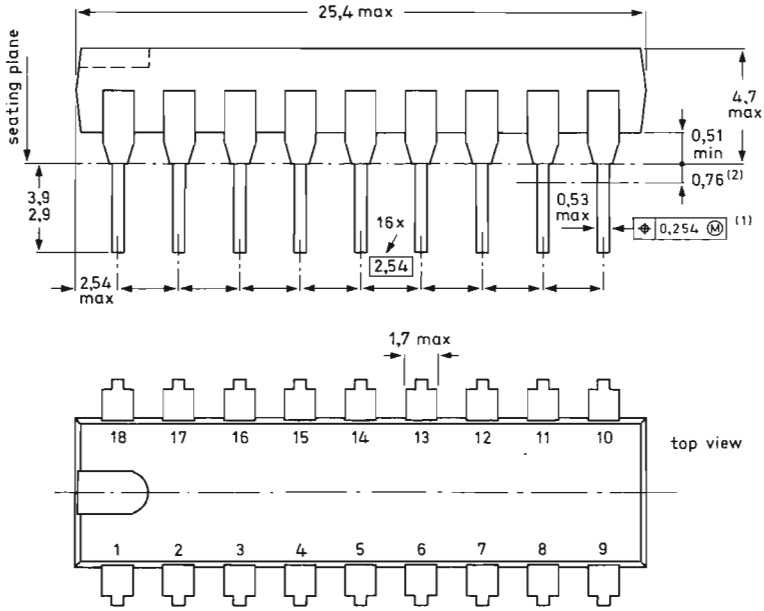


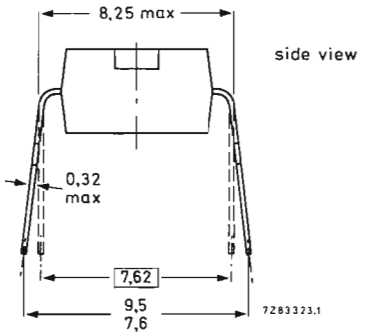
Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102G)





⊕ Positional accuracy.

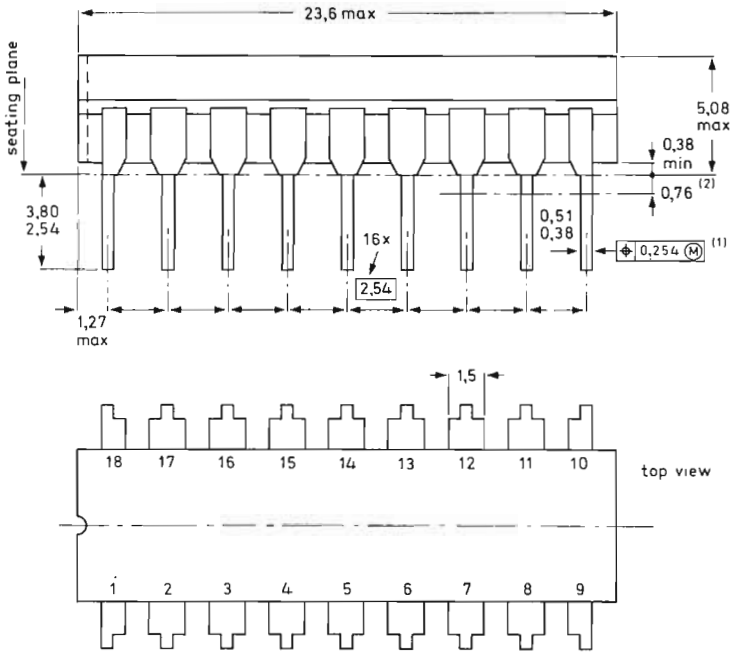
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

18-LEAD DUAL IN-LINE; CERAMIC (SOT-133)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3322 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- All inputs with pull-up/pull-down (except CE).
- 23-digit capacity for redial operation.
- Circuit reset for line power breaks; $\geq$ 160 ms.
- Dialling pulse frequency: 10 Hz.
- Test pulse frequency: 932 Hz.
- Hold facility for lengthening the inter-digit period.
- Memory overflow possibility (with internally disabled redial.
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3322P: 18-lead DIL; plastic (SOT-102G).
PCD3322D: 18-lead DIL; ceramic (SOT-133).

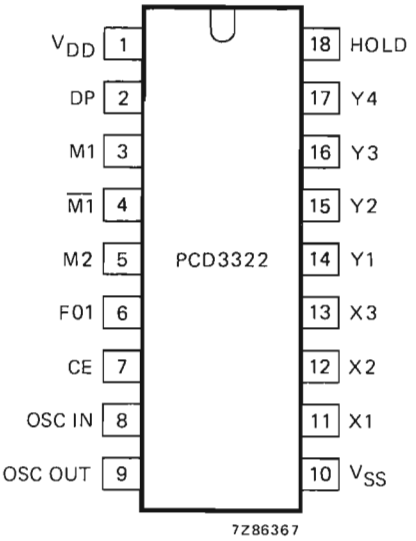


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

6	F01	the dialling pulse frequency is defined by the logic state of this input
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks.
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	
18	HOLD	interrupts dialling after completion of the current digit or immediately following an inter-digit pause (t_{id}); further keyboard data will be accepted

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence
4	$\overline{M1}$	inverted output of M1
5	M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

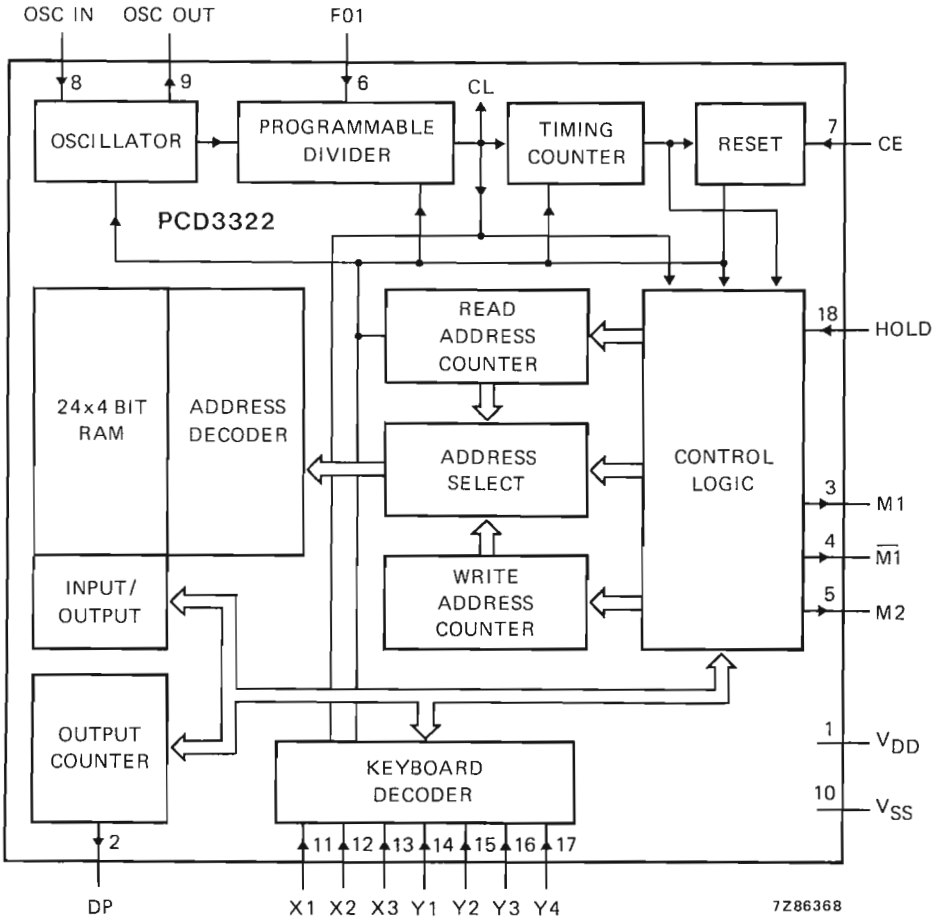


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3322 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set by input F01 to provide one of two chip system clocks; the 'normal' clock frequency (F01 = LOW) and the test frequency (F01 = HIGH).

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

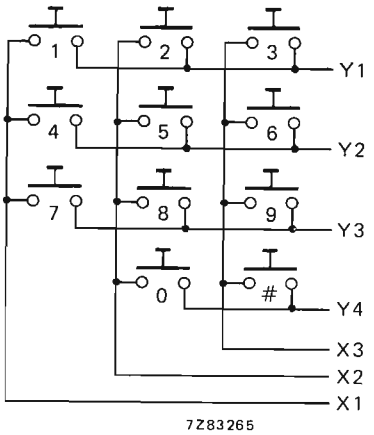
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig.3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored in the RAM and converted into correctly timed dialling pulses.



Redial.

Fig. 3 Single contact keyboard.

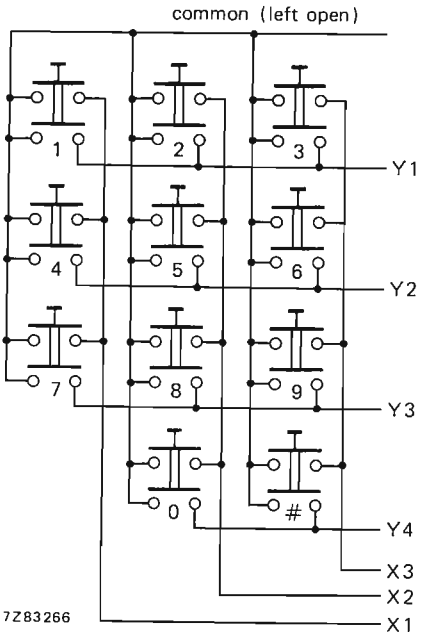


Fig. 4 Double contact keyboard.

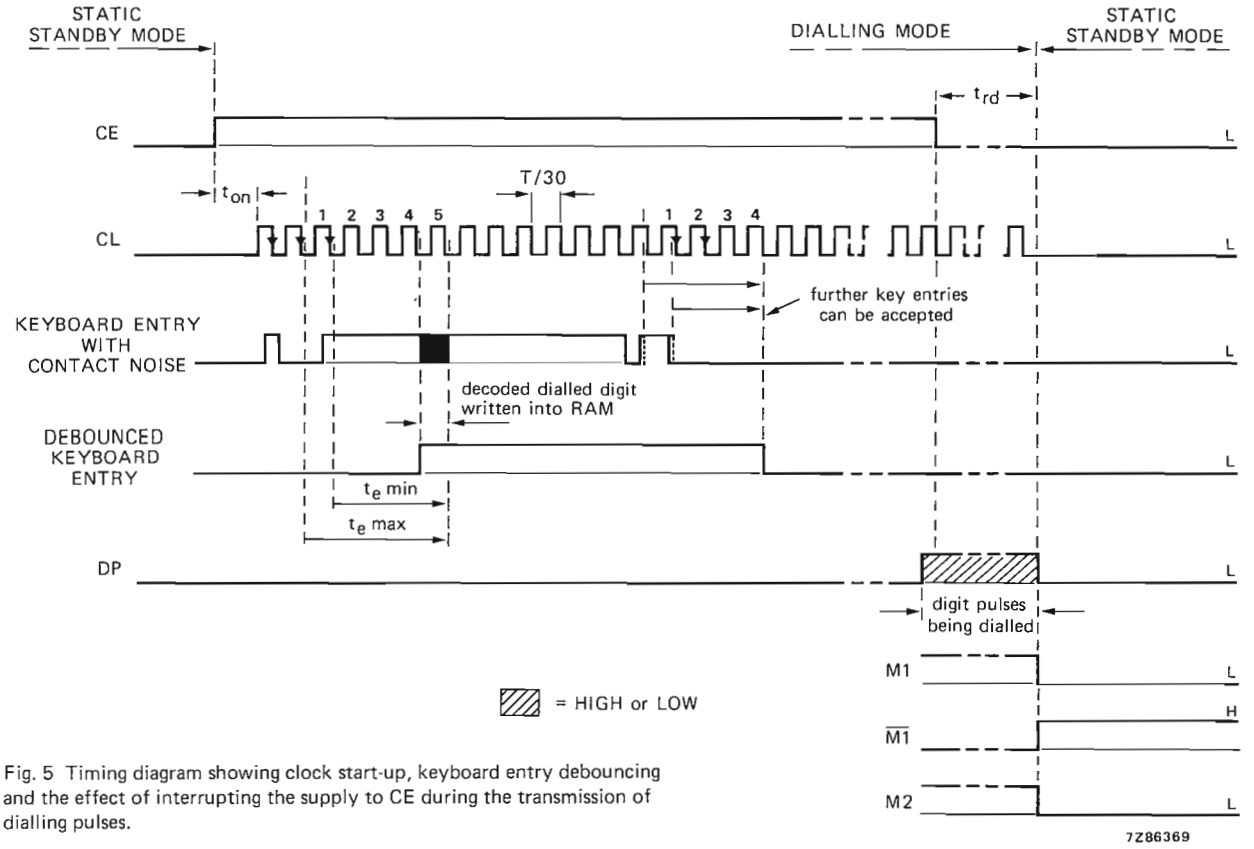


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL is an internal signal.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse-generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

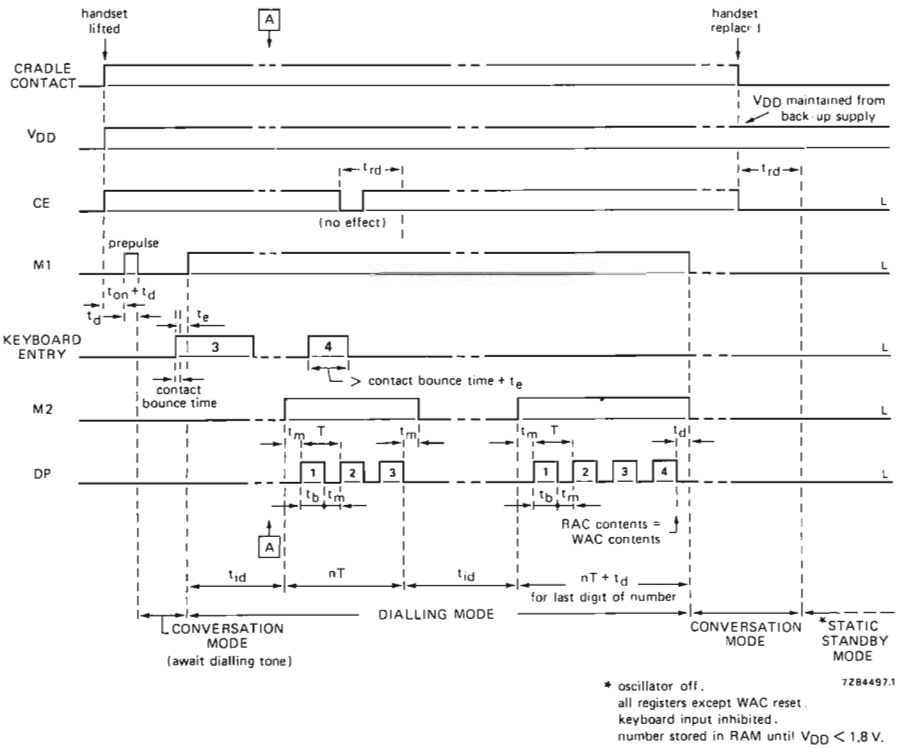


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts).

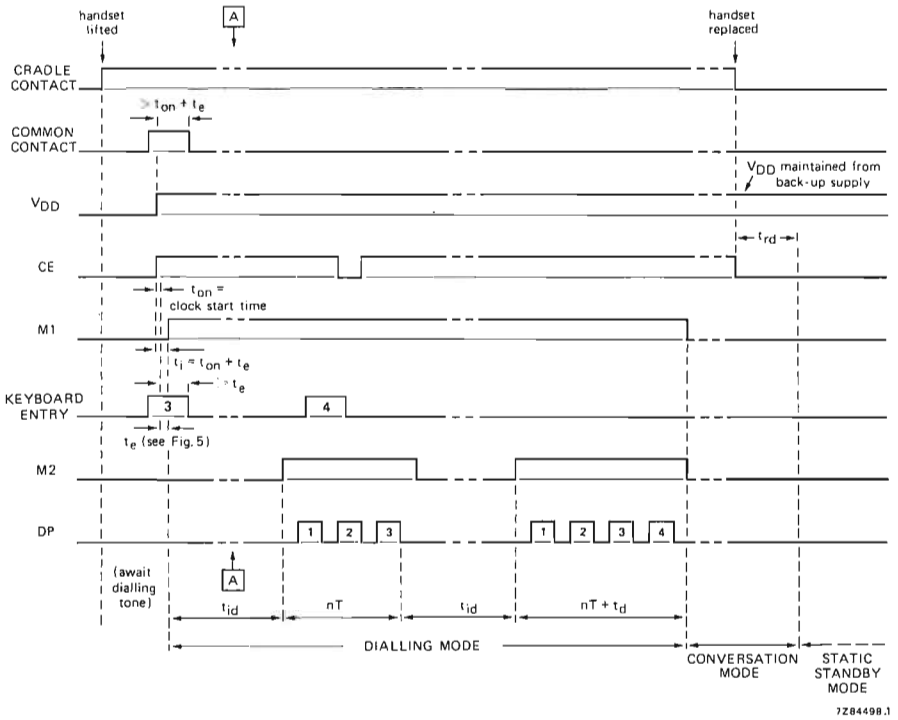


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

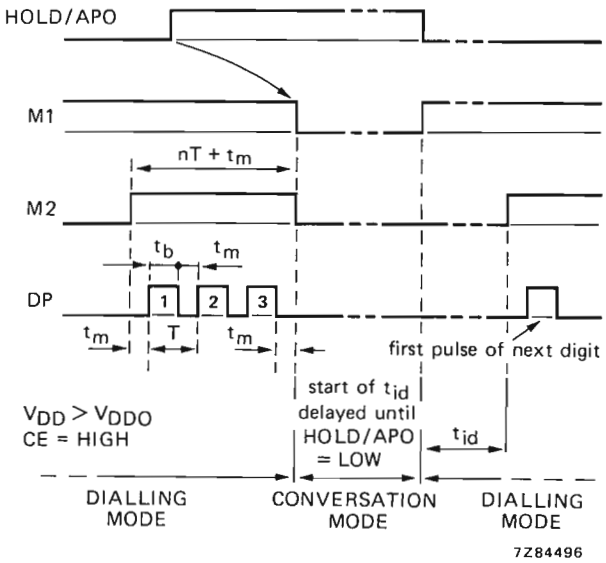


Fig. 8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to + 70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	—	6	V	T_{amb} = −25 to + 70 °C
Operating supply current	I_{DD}	—	40	—	μA	CE = HIGH; notes 2, 3
	I_{DD}	—	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	—	1	5	μA	CE = LOW; note 2
	I_{DDO}	—	—	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to + 70 °C
Input voltage LOW	V_{IL}	—	—	0,3 V_{DD}		1,8 V ≤ V_{DD} ≤ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	—	—		1,8 V ≤ V_{DD} ≤ 6 V
Input leakage current; CE LOW	$-I_{IL}$	—	—	50	nA	CE = LOW
HIGH	I_{IH}	—	—	50	nA	CE = HIGH
Pull-down input current F01, HOLD	I_{IH}	30	100	300	nA	$V_I = V_{DD}$
Matrix keyboard operation						
Keyboard current	I_K	—	10	—	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	—	—	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	—	—	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	—	—	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	—	—	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	—	—	0,7	mA	$V_I = V_{SS}$
Output sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
Output source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

TIMING DATA I

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz; R_{Smax} = 100 Ω

	symbol	min.	typ.	max.		conditions
Clock start-up time	t_{on}	–	4	–	ms	Figs 6, 7; note 1
Initial data entry time ($t_i = t_{on} + t_e$)	$t_{i\,min}$	–	18	–	ms	F01 = LOW } Fig. 7
	$t_{i\,max}$	–	4	–	ms	F01 = HIGH }

TIMING DATA II (exact values)

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

	symbol	F01 = LOW (dialling)	F01 = HIGH (testing)		conditions
Dialling pulse frequency	f_{DP}	10,13	932,2	Hz	note 2
Dialling pulse period; $1/f_{DP}$	T_{DP}	98,7	1,073	ms	Figs 6, 7
Prepulse duration; 1/3 x T_{DP}	t_d	33	0,358	ms	Figs 6, 7
Inter-digit pause; 8 x T_{DP}	t_{id}	790	8,58	ms	Figs 6, 7
Break time; 3/5 x T_{DP}	t_b	59,2	0,644	ms	Fig. 6
Make time; 2/5 x T_{DP}	t_m	39,5	0,429	ms	Fig. 6
Debounce time					
min. 4/30 x T_{DP}	$t_{e\,min}$	13,2	0,143	ms	Fig. 5
max.; 1/6 x T_{DP}	$t_{e\,max}$	16,5	0,179	ms	Fig. 5
Reset delay time; 1,6 x T_{DP}	t_{rd}	158	1,7	ms	Figs 5, 6, 7

Notes

1. Stray capacitance between pins 8 and 9 < 3 pF.
2. Exactly 10 Hz and 920 Hz respectively when a 3,5328 MHz crystal is used.

TYPICAL CURVES

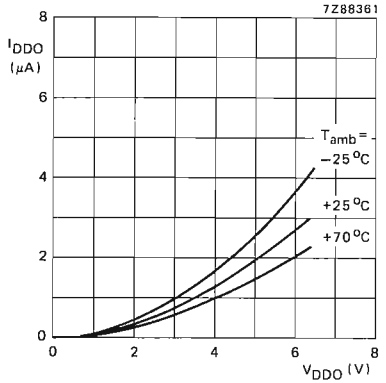


Fig. 9 Standby supply current as a function of standby supply voltage.

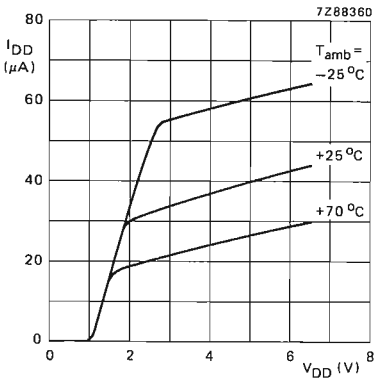


Fig. 10 Operating supply current as a function of operating supply voltage.

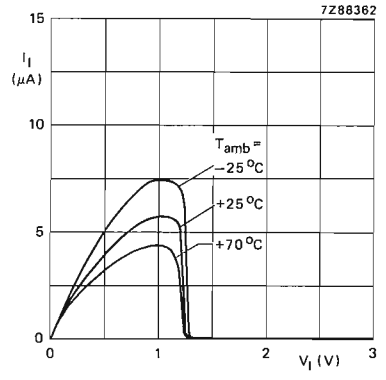


Fig. 11 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

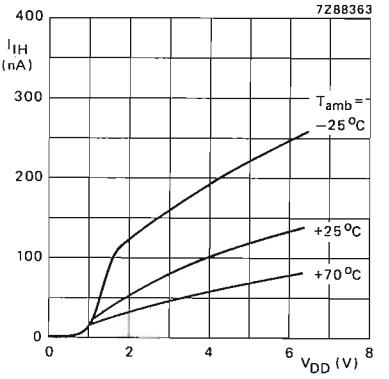


Fig. 12 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

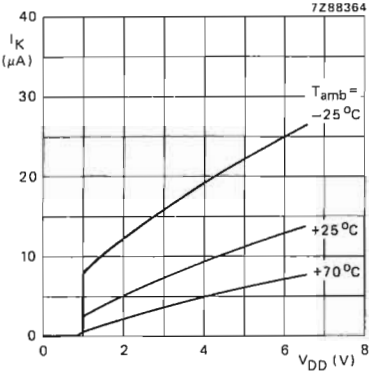


Fig. 13 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

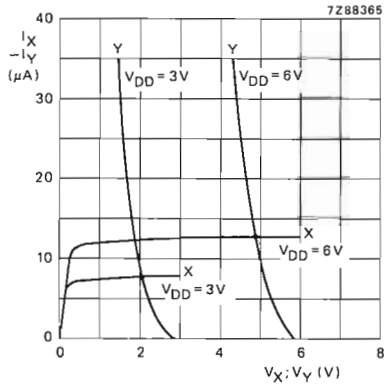


Fig. 14 Keyboard input characteristics at T_{amb} = 25 °C.

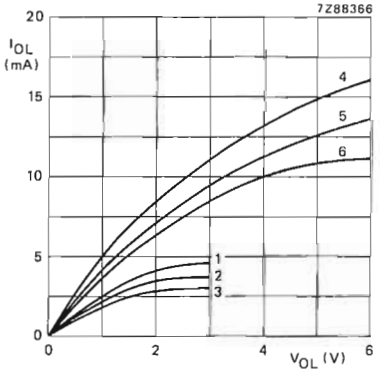


Fig. 15 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M2 and DP.

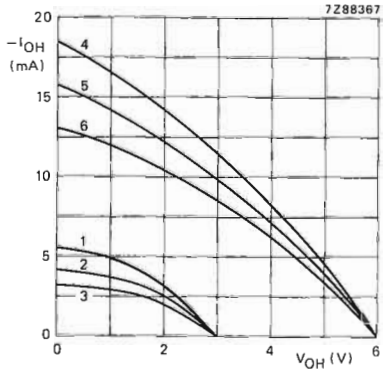
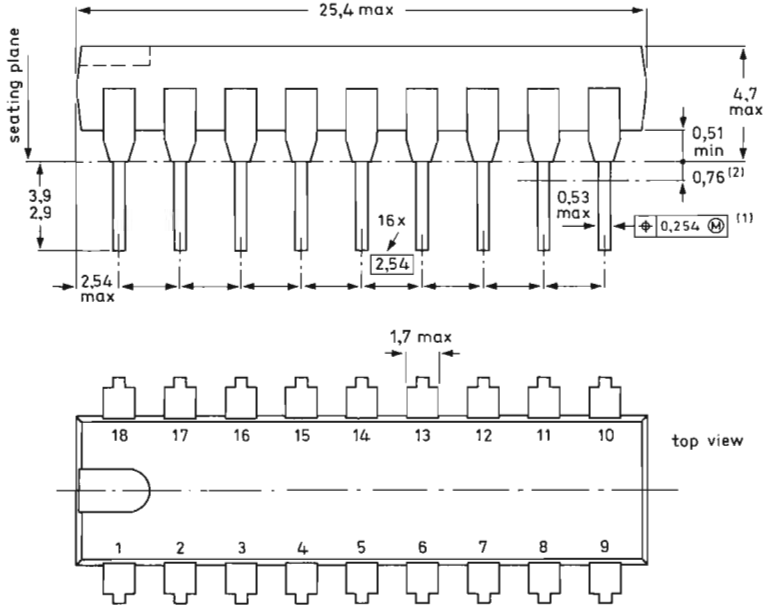


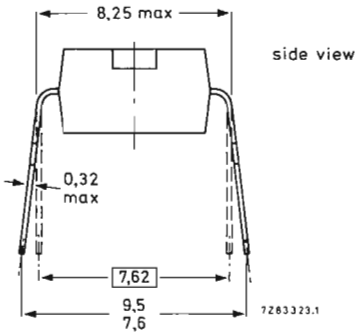
Fig. 16 Output (P-channel) source characteristics for M1, $\overline{M1}$, M2 and DP.

Curves for Figs 15 and 16

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102G)





⊕ Positional accuracy.

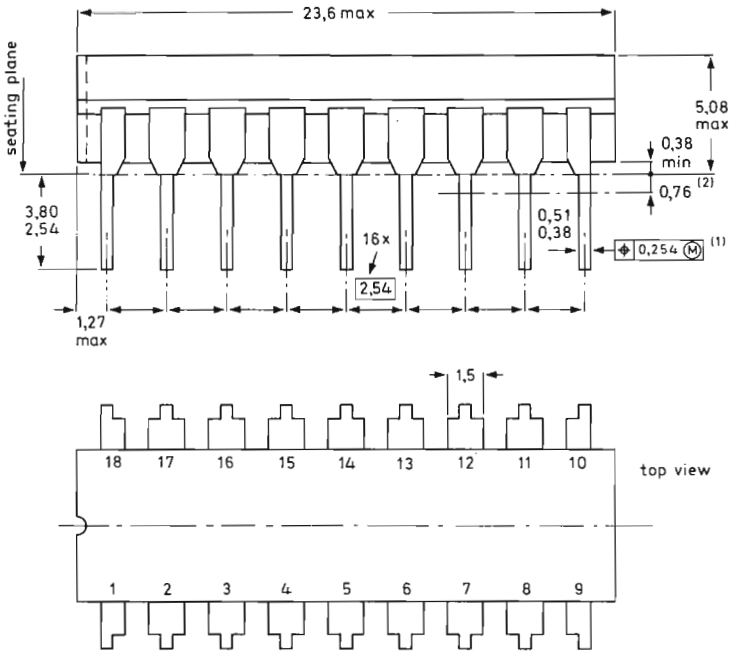
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

18-LEAD DUAL IN-LINE; CERAMIC (SOT-133)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3323 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3323 can regenerate access pauses during redial. During the original entry, access pauses are stored either automatically or via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems.

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Selectable inter-digit pause (t_{id}); 8 or 9 times the pulse period (T_{DP}).
- Hold facility for lengthening the inter-digit period.
- Selectable circuit reset for line power breaks; > 160 ms or > 320 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s or 6 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3323P : 28-lead DIL; plastic (SOT-117D).
PCD3323D: 28-lead DIL; ceramic (SOT-135).
PCD3323T: 28-lead flat pack; plastic (SO-28; SOT-136A).

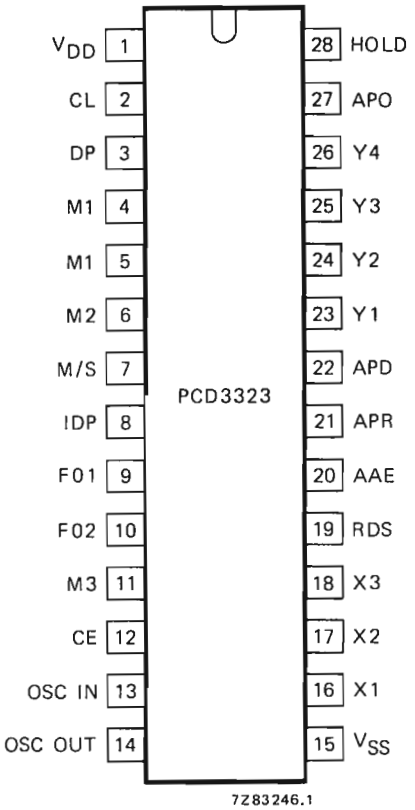


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
15	V_{SS}	negative supply

Inputs

7	M/S	controls the mark-to-space ratio of the line pulses
8	IDP	Inter-Digit-Pause; this occurs before each digit appears at the line output; the duration (t_{id}) can be controlled with this pin
9	F01	the dialling pulse frequency is defined by the logic state of these two inputs
10	F02	
12	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
16	X1	column keyboard inputs with pull-down on chip
17	X2	
18	X3	
19	RDS	Reset Delay Selection; delay select for chip enable (CE) activity.

20	AAE	Automatic Access Pause Enable; AAE = HIGH: the circuit generates a maximum of two automatic pauses; AAE = LOW: only manual pauses (via keyboard) are possible
21	APR	Access Pause Reset; when any external circuit makes APR = HIGH, a current access pause will be terminated
22	APD	Access Pause Delay; selects the maximum duration of an access pause if no external Access Pause Reset appears.
23	Y1	row keyboard inputs with pull-up on chip
24	Y2	
25	Y3	
26	Y4	
28	HOLD	interrupts dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted

Outputs

2	CL	output of the internal system clock; external forcing is possible for frequencies not selectable with F01/F02
3	DP	Dialling Pulse; drive of the external line switching transistor or relay
4	$\overline{M1}$	Muting; normally used for muting during the dialling sequence
5	M1	inverted output of M1
6	M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause
11	M3	AND function, with $\overline{DP}$ and M1 as input, for direct drive of a switching transistor for dialling pulses and muting
27	APO	Access Pause Output; this output will go HIGH when an access pause code is read from the memory during pulsing.

Oscillator

13	OSC IN	input and output of the on-chip oscillator
14	OSC OUT	

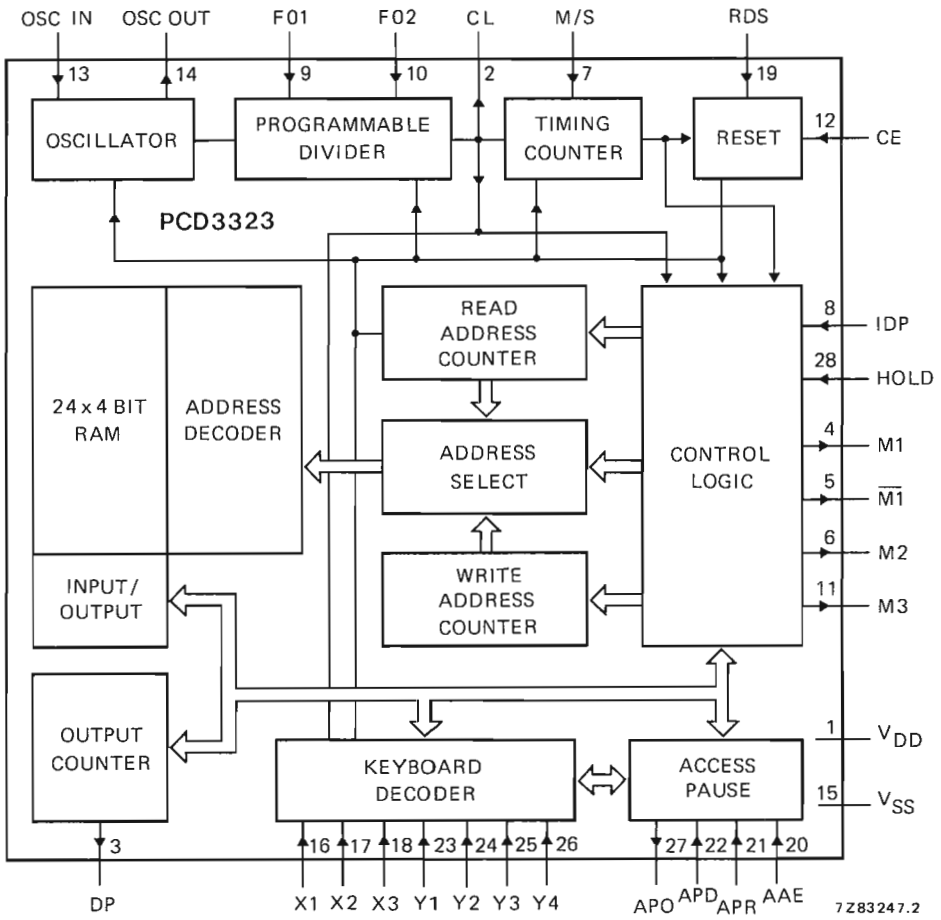


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3323 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.
The system clock is available on pin CL and can be used for external logic. External forcing of CL is possible for frequencies which are not selectable with F01/F02.
Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced. The t_{rd} pulse duration is selected by the RDS input.

Debouncing keyboard entries

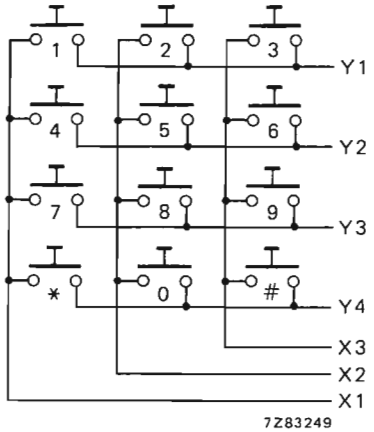
The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC reprents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP.

If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3323. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

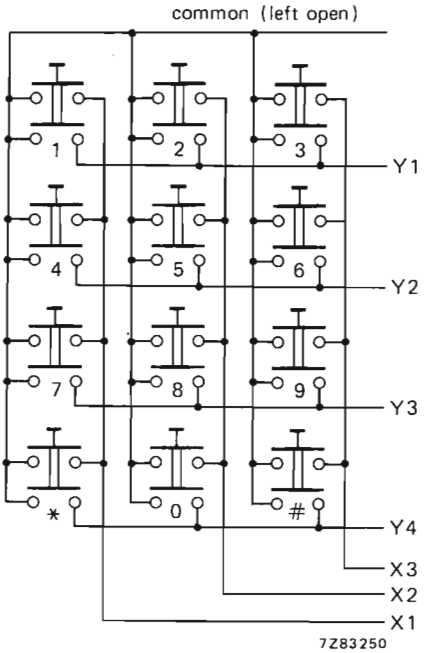


Fig. 4 Double contact keyboard.

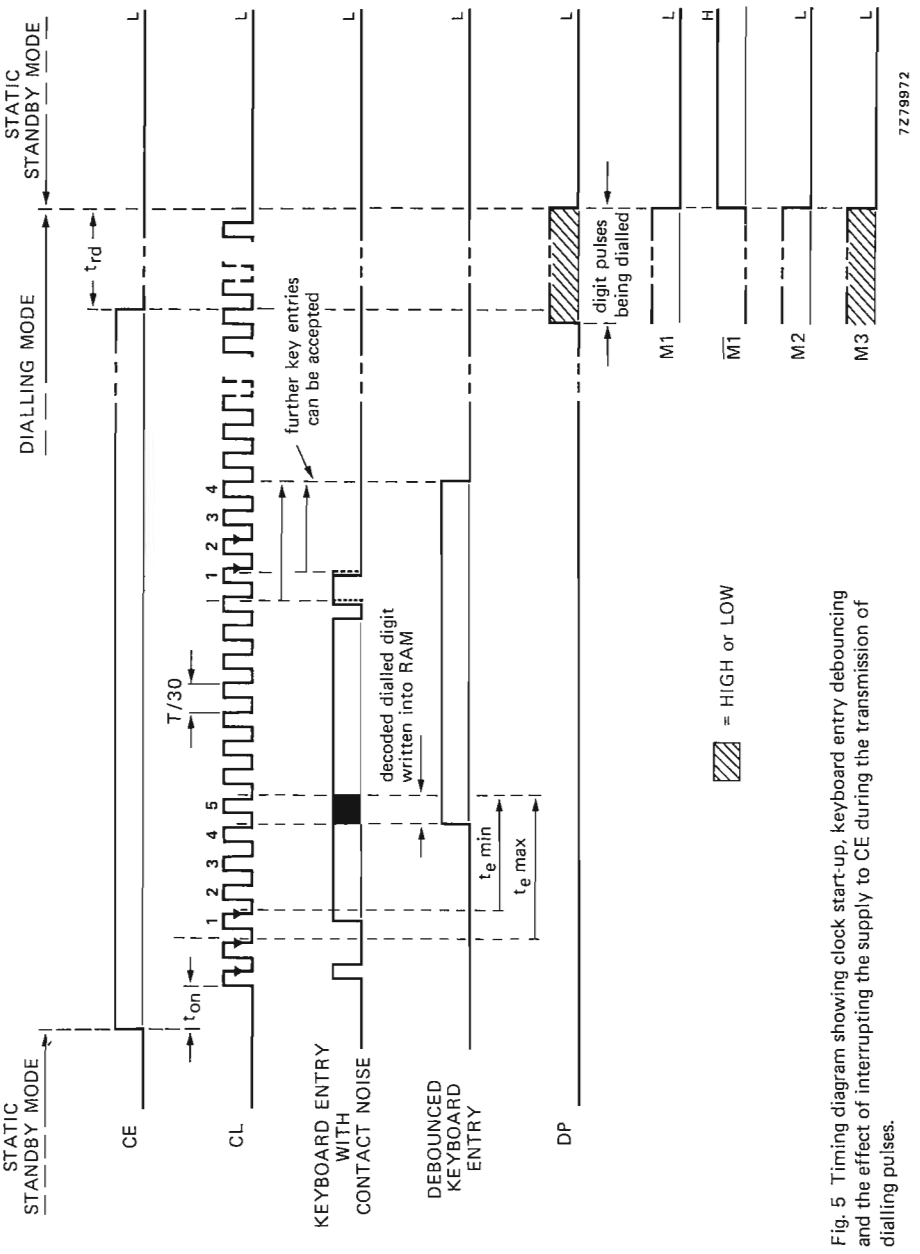


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 or 3,2 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

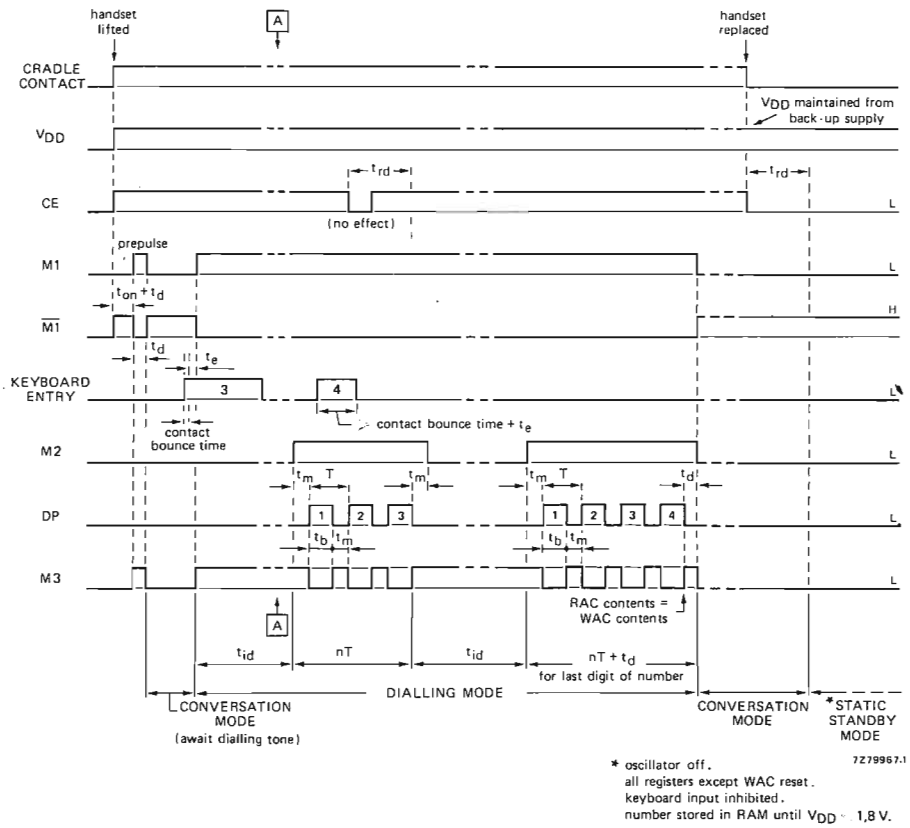


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts).

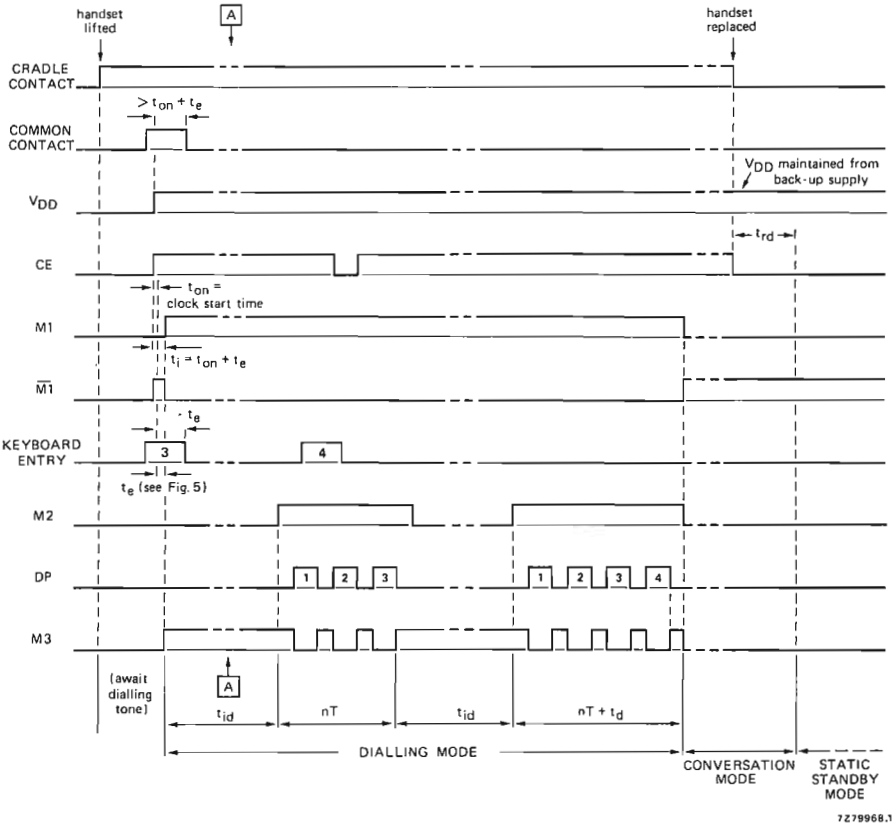


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

HOLD can be controlled by the Access Pause Output (see next section).

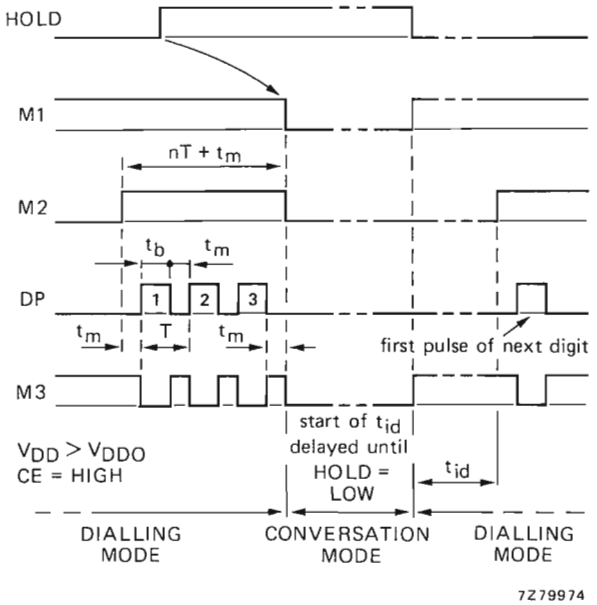


Fig. 8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

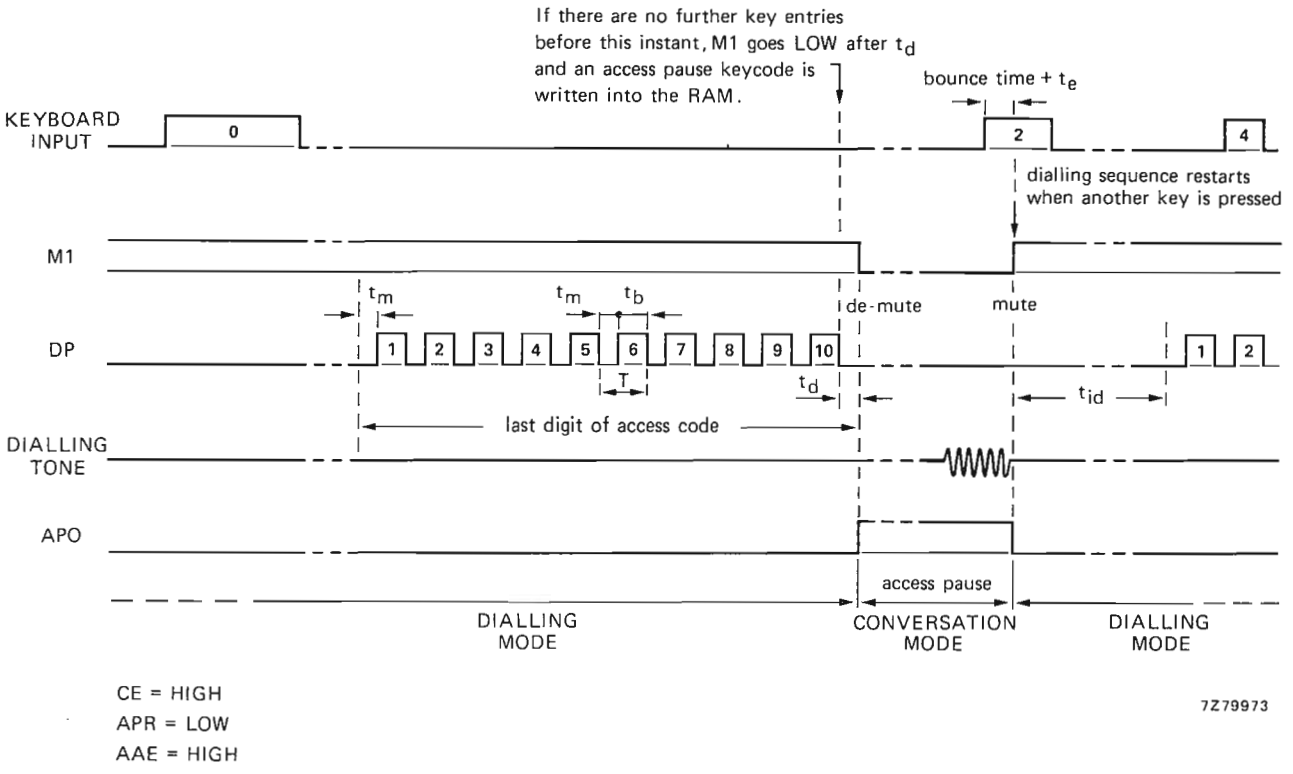


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (APO) will go HIGH as soon as an access pause code is read from the RAM. This can be used to make HOLD = HIGH, thereby interrupting dialling until HOLD is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause.

Access pause codes can be stored in two ways:

- *Manually,* with AAE and APR both LOW. In this case access pause codes can only be stored by pressing the access pause key (★) between entering the trunk exchange code and the subscriber code, or at any other moment an access pause is required. The number of access pauses that can be inserted in this manner is only limited by the capacity of the RAM (digits + access pauses ⩽ 23).
- *Automatically,* with AAE = HIGH and APR = LOW (see Fig. 9). An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Up to two access pauses can be entered into the RAM in this manner. Alternatively, the access pause key can still be pressed to insert (more) access pauses manually.

During redial, access pauses will be regenerated only if APR = LOW and with APO connected to HOLD; they can be terminated in three ways (see Fig. 10 and next page).

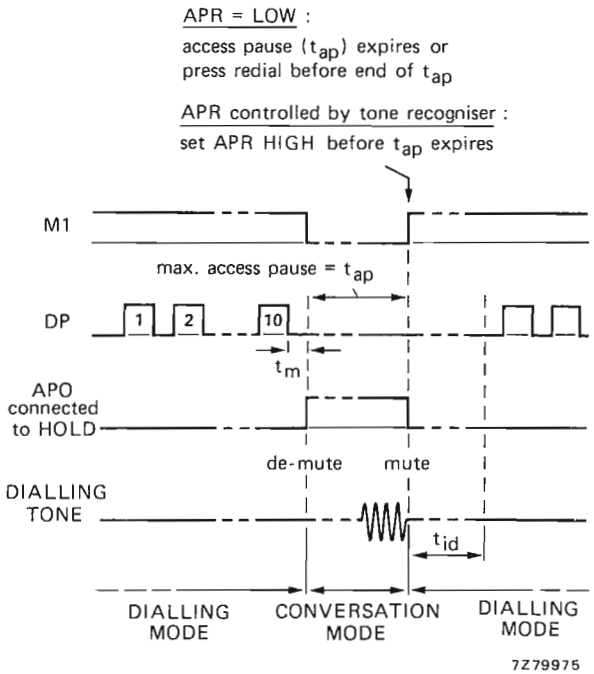


Fig. 10 Timing diagram showing Access Pause Reset for APR = LOW or APR is controlled by tone recogniser.

Three methods of terminating an access pause:

1. Automatically, if the built-in time t_{ap} expires; APO then goes LOW; t_{ap} can be set to one of two values with the Access Pause Delay (APD) select input.
2. Manually, by pressing the redial key before t_{ap} expires.
3. By making APR = HIGH before t_{ap} expires, with an external tone recogniser (see Fig. 11).

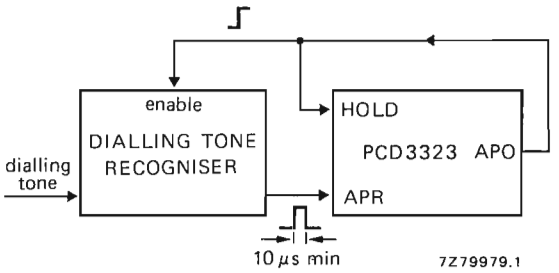


Fig. 11 Circuit for automatic termination of an access pause during redialling by using a tone recogniser to set APR to HIGH for more than 10 μs.

Access pauses longer than t_{ap} can be obtained by connecting APO to HOLD via a latching device. Figure 12 shows a tone recogniser circuit, which automatically terminates access pauses upon receipt of the access tone, whether this is before or after t_{ap} expires.

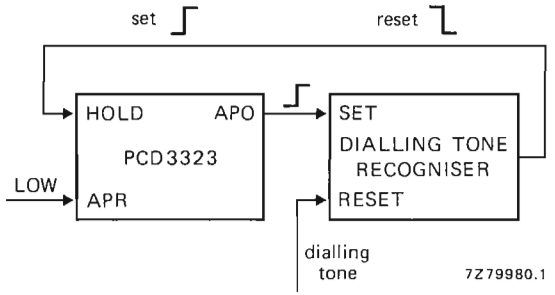


Fig. 12 Circuit for automatically shortening or lengthening an access pause under the control of a tone recogniser. For timing diagram see Fig. 13.

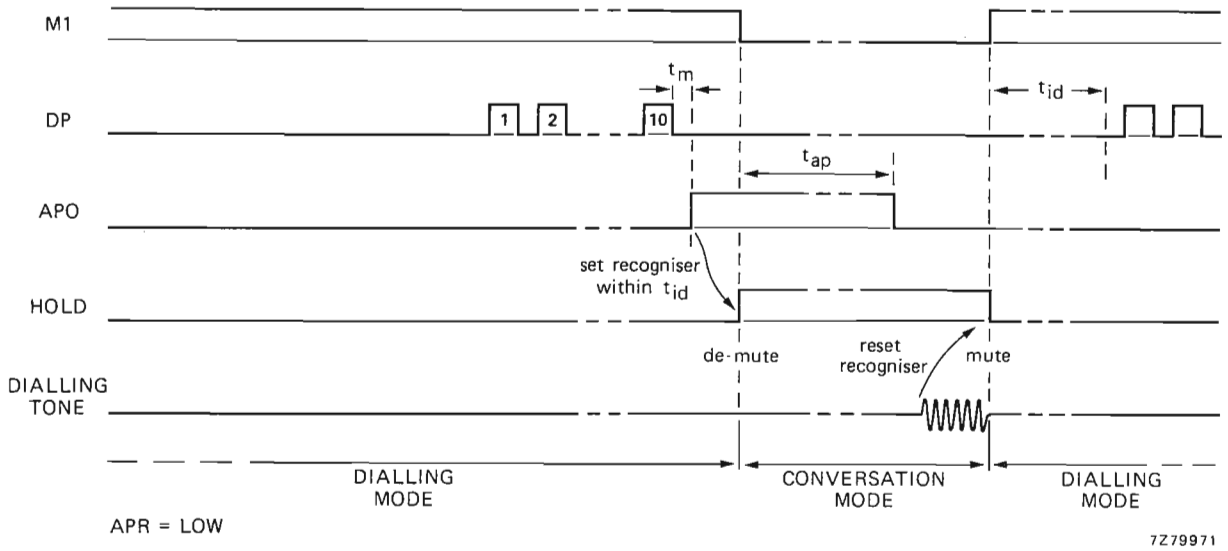


Fig. 13 Timing diagram showing automatic shortening or lengthening an access pause; for the circuit see Fig. 12.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	T_{amb} = −25 to + 70 °C
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to + 70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to + 70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ≤ V_{DD} ≤ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ≤ V_{DD} ≤ 6 V
Input leakage current; CE						
LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S, APR	$-I_{IL}$	30	100	300	nA	$V_I = V_{SS}$
Pull-down input current IDP, F01, F02, HOLD, AAE, ADP, RDS	I_{IH}	30	100	300	nA	$V_I = V_{DD}$
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	$V_I = V_{SS}$

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 13 and 14 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, $\overline{M1}$, M2, M3, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Outputs CL, APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 3,58 MHz

	symbol	min.	typ.	max.		conditions
Clock start-up time	t_{on}	–	4	–	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note)
APR-hold time	t_{APRH}	10	–	–	μs	see Fig. 11

Note: stray capacitance between pins 13 and 14 ≤ 3 pF.

TIMING DATA (continued)

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		
		V_{F02}	LOW	HIGH	HIGH	LOW		conditions (note 4)
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	932,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	IDP = L; n.c.
	$9 \times T_{DP}$	t_{id}	888	579	463	9,65	ms	IDP = H
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	RDS = L; n.c.
	$3,2 \times T_{DP}$	t_{rd}	316	206	165	3,43	ms	RDS = H
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	APD = L; n.c.
	$64 \times T_{DP}$	t_{ap}	6,32	4,12	3,30	0,069	s	APD = H
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min.	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3: 2.
3. Mark-to-space ratio: 2: 1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.

TYPICAL CURVES

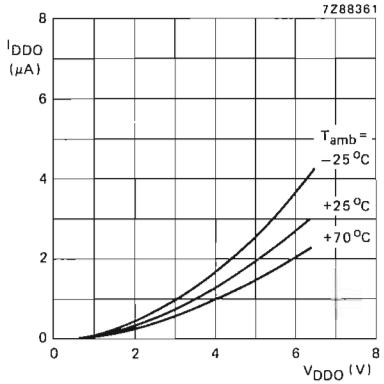


Fig. 14 Standby supply current as a function of standby supply voltage.

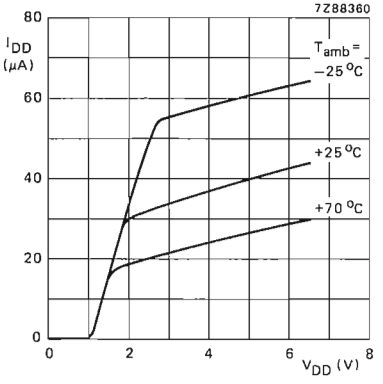


Fig. 15 Operating supply current as a function of operating supply voltage.

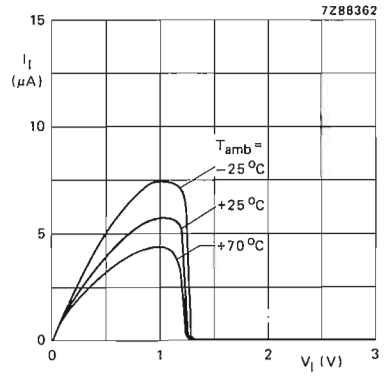


Fig. 16 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

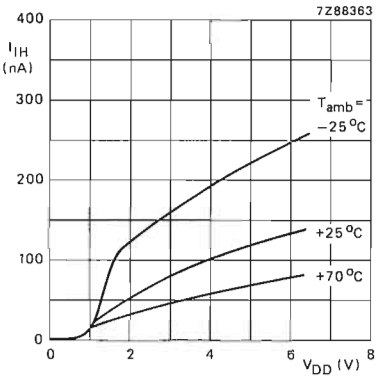


Fig. 17 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

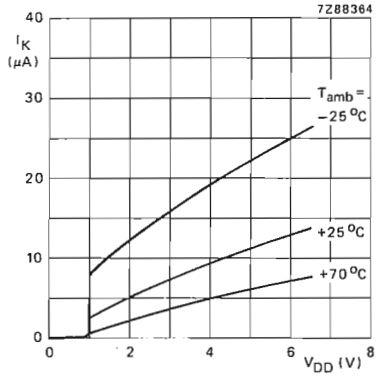


Fig. 18 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

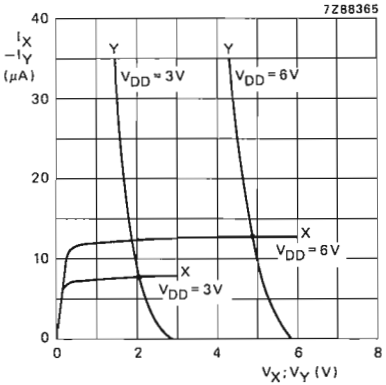


Fig. 19 Keyboard input characteristics at T_{amb} = 25 °C.

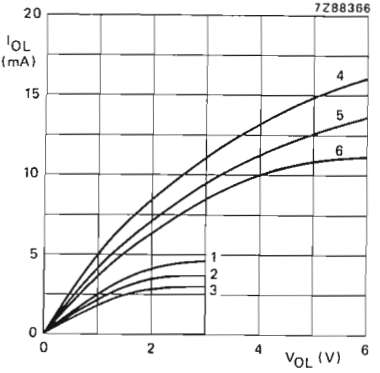


Fig. 20 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M2, M3 and DP.

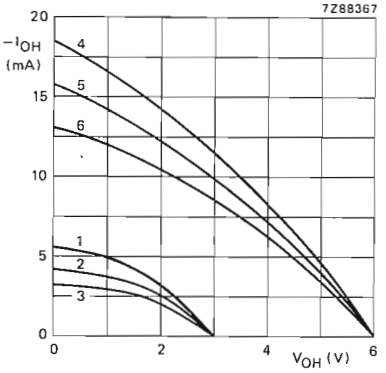
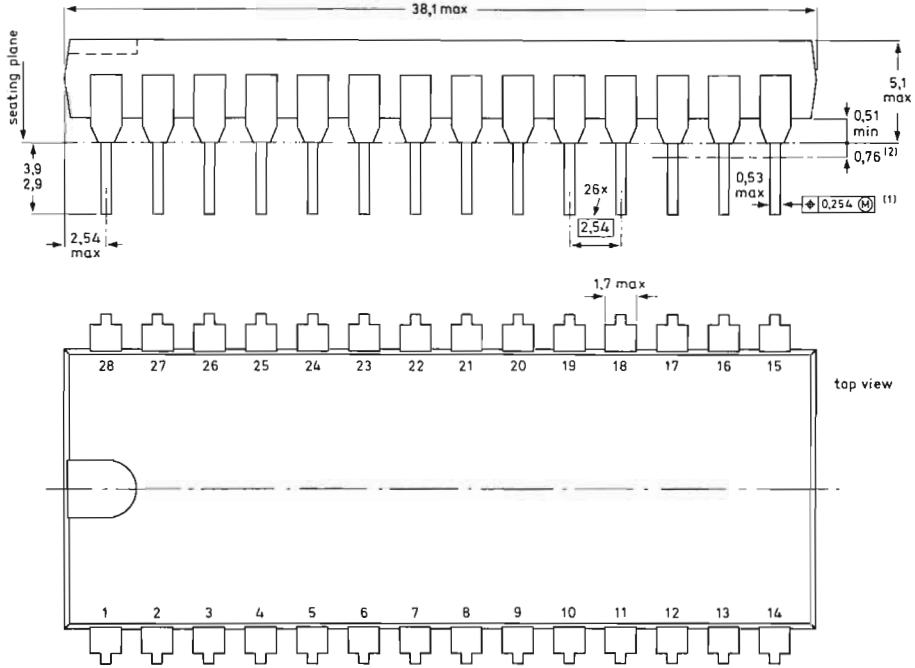


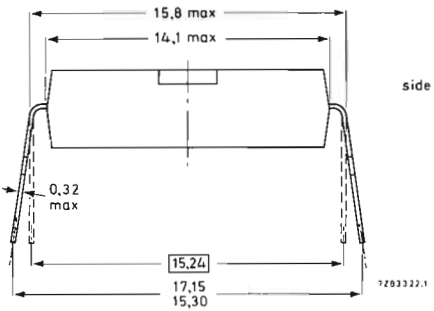
Fig. 21 Output (P-channel) source characteristics for M1, $\overline{M1}$, M2, M3 and DP.

Curves for Figs 20 and 21

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117D)





⊕ Positional accuracy.

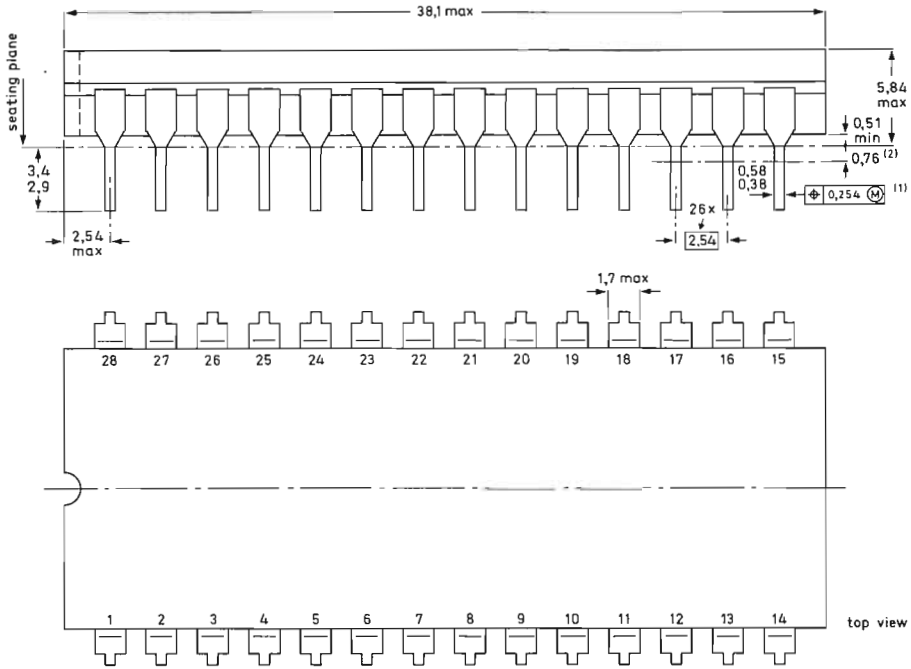
Ⓜ Maximum Material Condition.

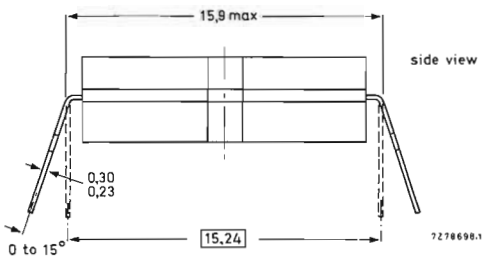
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; CERAMIC (SOT-135)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

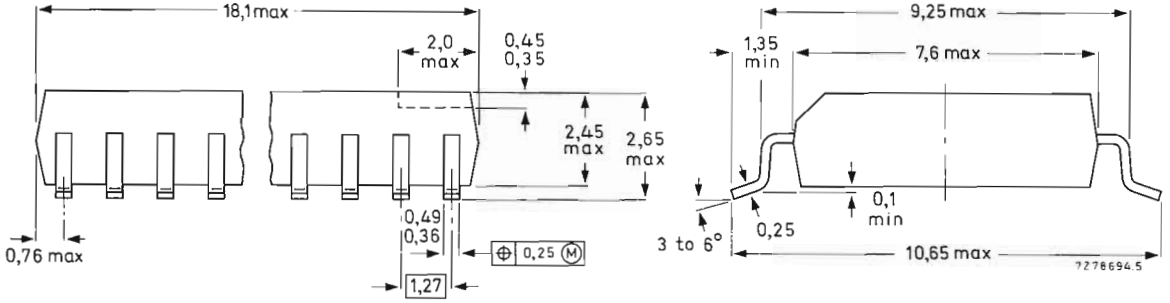
(2) Lead spacing tolerances apply from seating plane to the line indicated.

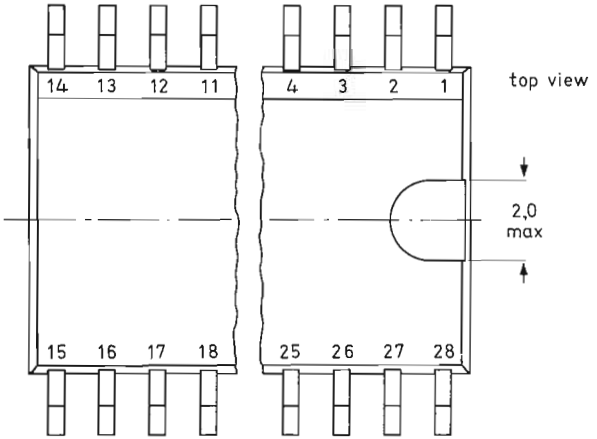
Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

28-LEAD FLAT PACK; PLASTIC (SO-28; SOT-136A)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

See next page.

SOLDERING

The reflow solder technique

The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3324 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3324 can regenerate access pauses during redial. During the original entry, only one access pause is stored automatically or several via the keyboard. A regenerated access pause can be terminated during redial in three ways: automatically after a built-in time, or via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems. The PCD3324 is pin to pin compatible with the DF320 and the MT4320 (however, including additional functions).

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; > 160 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  automatically after 3 s (10 Hz dialling pulse frequency),
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINES

PCD3324P : 18-lead DIL; plastic (SOT-102G).
PCD3324D: 18-lead DIL; ceramic (SOT-133).

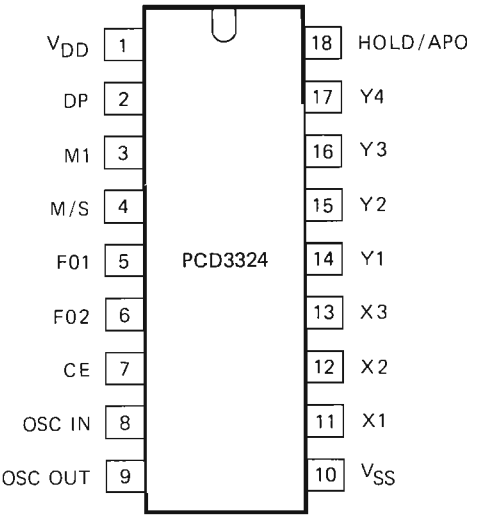


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

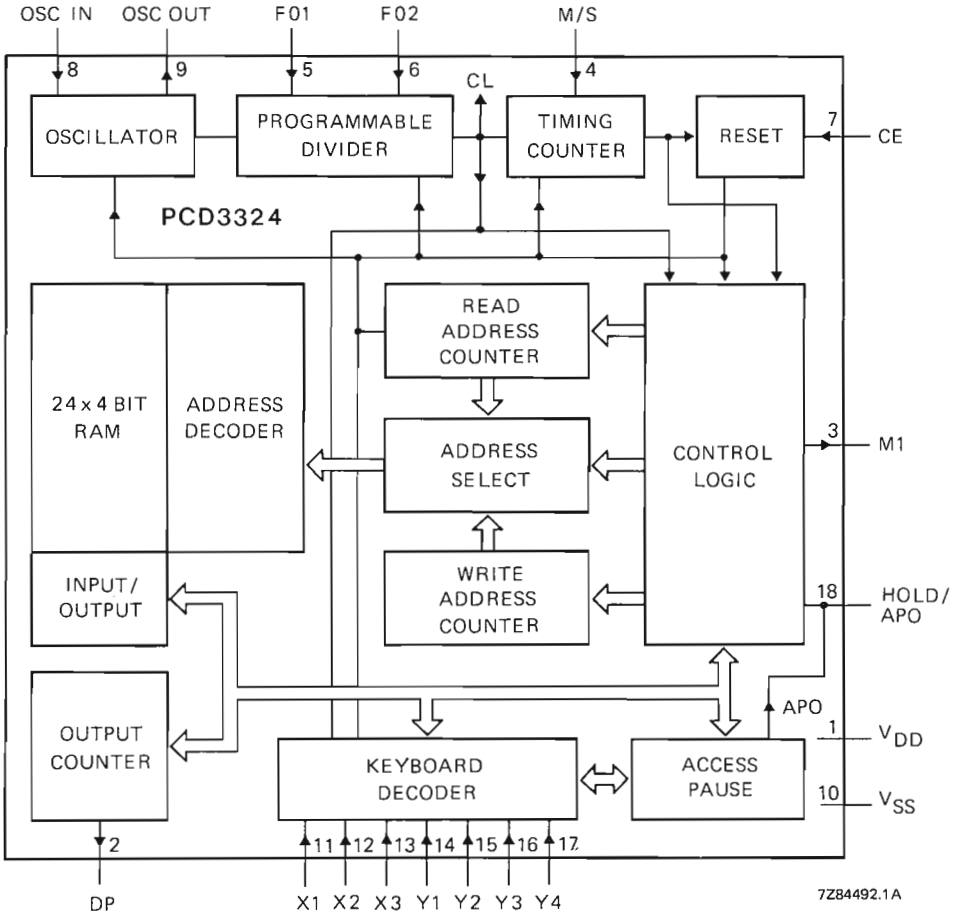


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the **PCD3324** is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

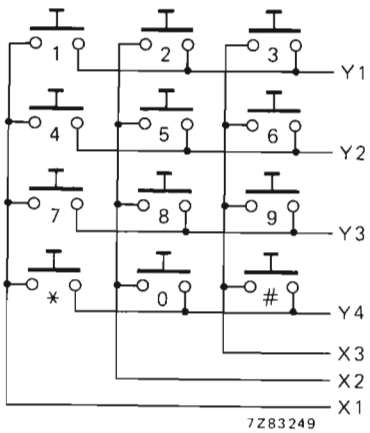
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3324. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

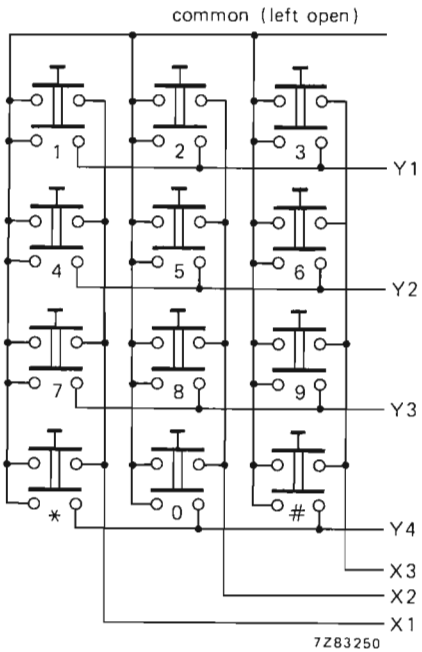


Fig. 4 Double contact keyboard.

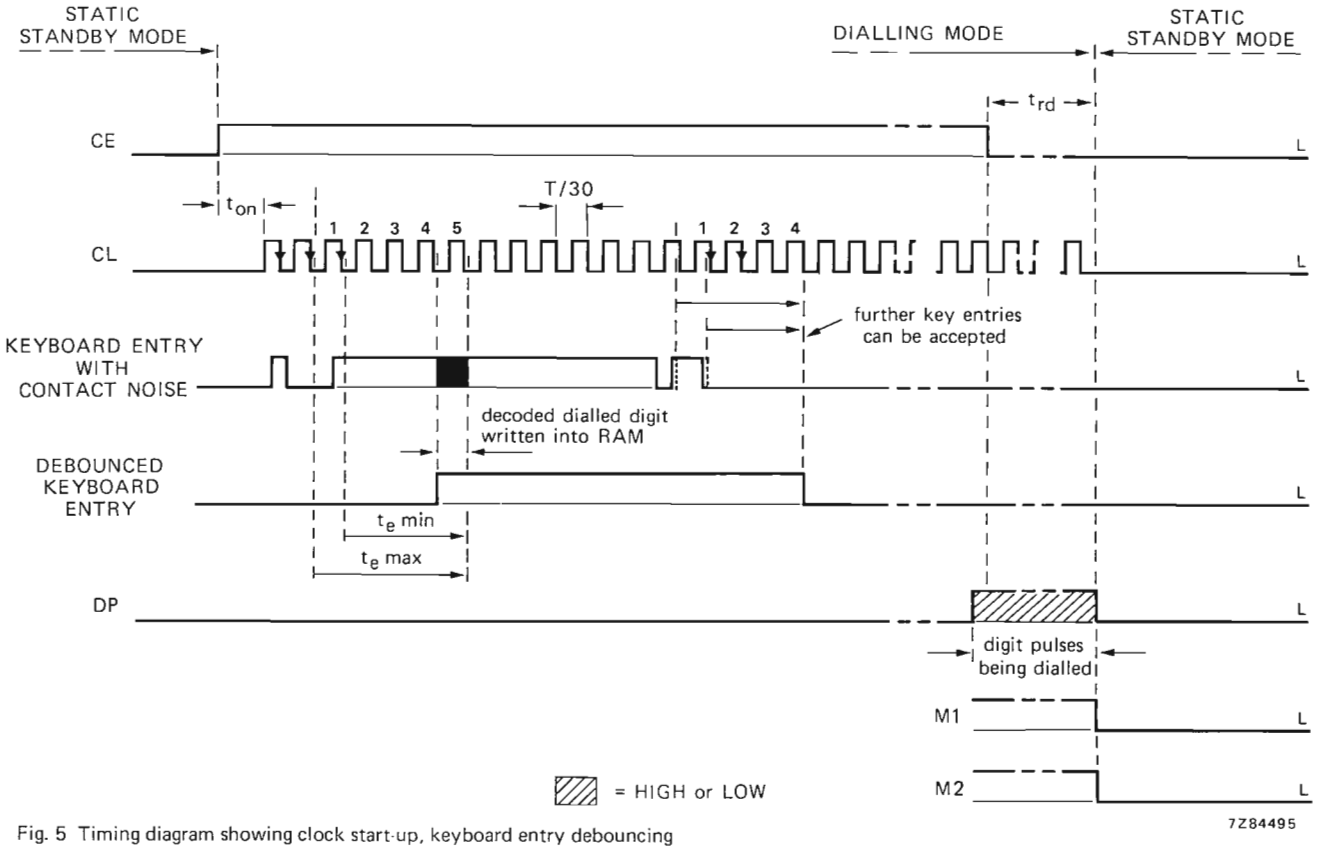


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.
N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

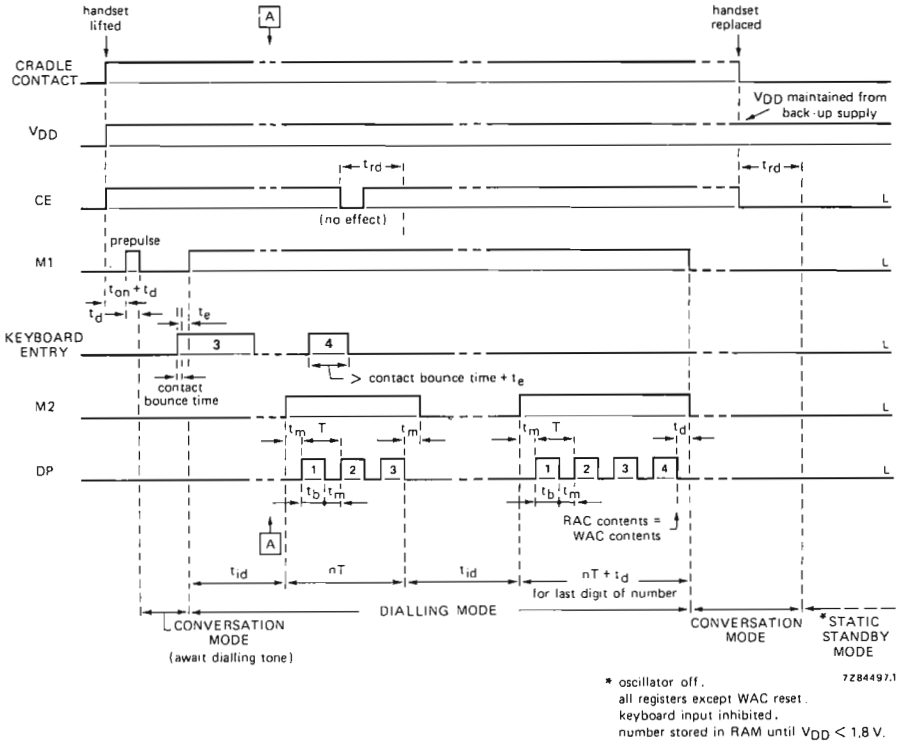


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

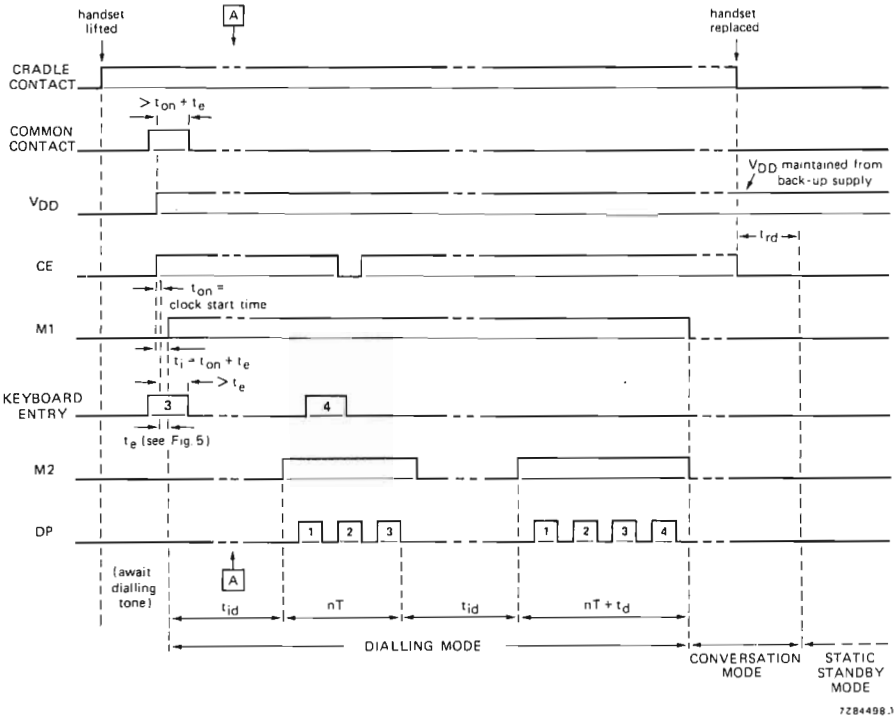


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

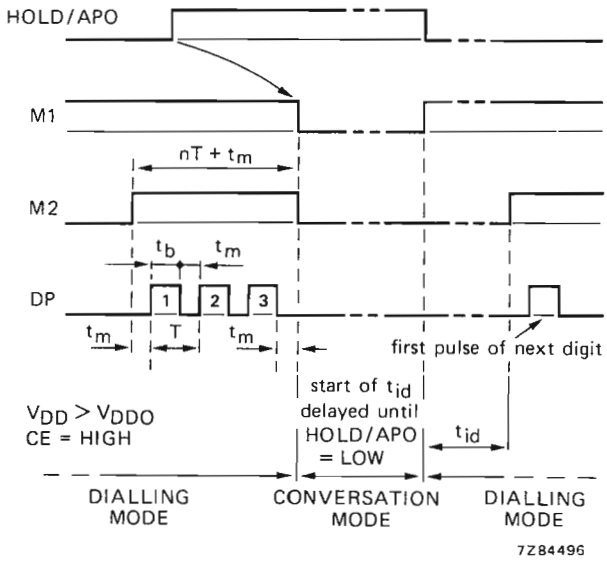


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

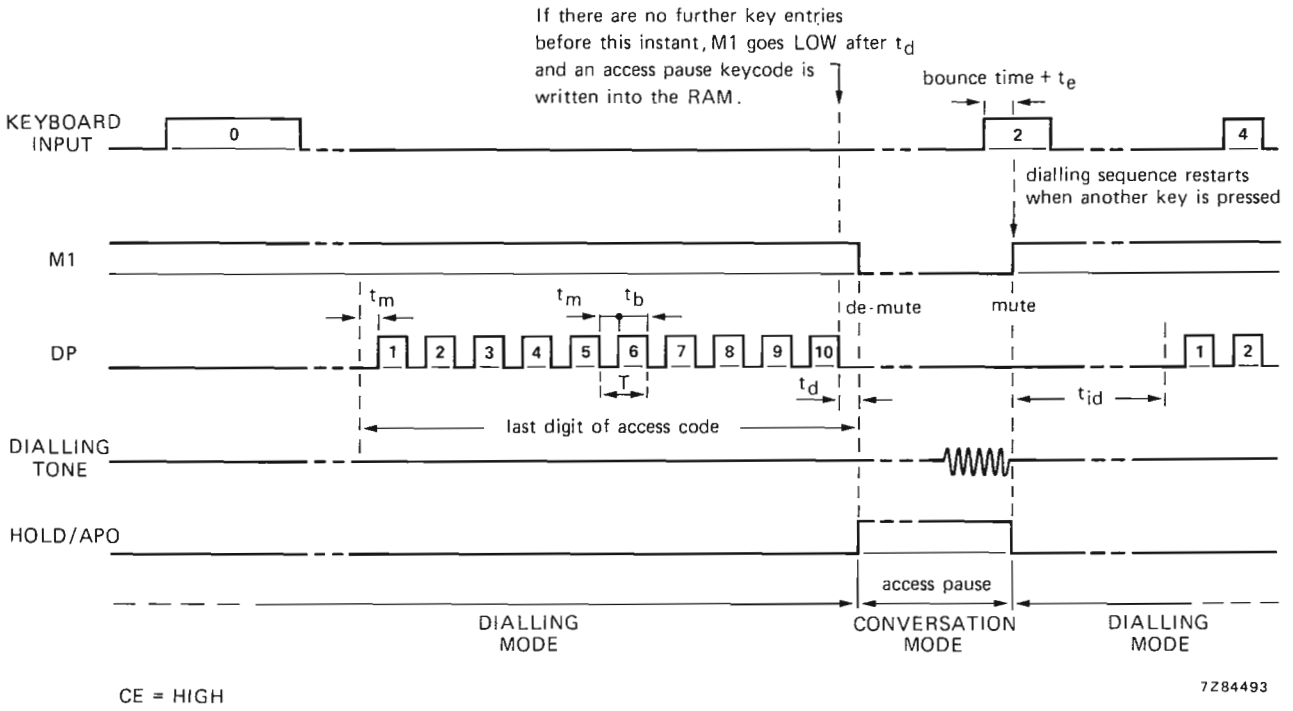
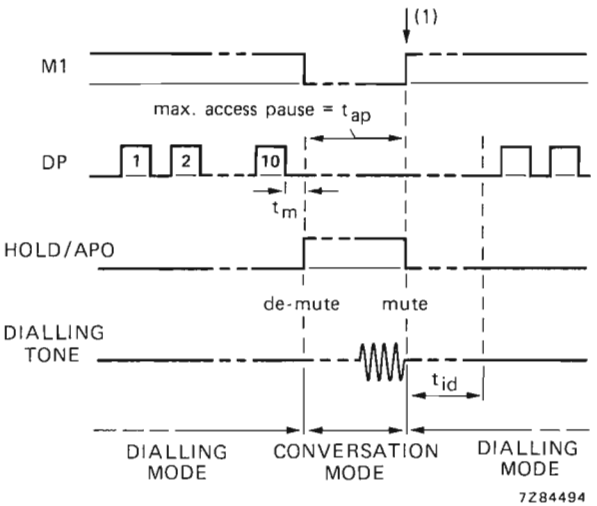


Fig. 9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO)will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is now automatically stored in the RAM during original entry, when M1 goes LOW, after all digits so far entered have been transmitted (see Fig. 6). This occurs between entering of the trunk exchange code and the subscriber code, whilst the access tone is available. Only one access pause can be entered into the RAM in this manner. Alternatively, the access pause key (★) can still be pressed to insert (more) access pauses manually (digits + access pauses ⩽ 23).
During redial, access pauses will be automatically regenerated.

Three methods of terminating an access pause:
1. Automatically, if the built-in time t_{ap} expires; HOLD/APO then goes LOW.
2. Manually, by pressing the redial key before t_{ap} expires.
3. With an external tone recogniser, by forcing HOLD/APO to LOW or HIGH respectively, for shortening or lengthening an access pause.



(1) a. Access pause (t_{ap}) expires or press redial before end of t_{ap}.

b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW before t_{ap} expires; access pause $< t_{ap}$
HOLD/APO forced to HIGH after t_{ap} expires; access pause $> t_{ap}$.

Fig. 10 Timing diagram showing Access Pause Reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	2	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ≤ V_{DD} ≤ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		conditions (note 4)
		V_{F02}	LOW	HIGH	HIGH	LOW		
		symbol				(test mode)		
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Access pause time	$32 \times T_{DP}$	t_{ap}	3,16	2,06	1,65	0,034	s	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	—	—	—	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 5)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. Mark-to-space ratio: 2:1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
5. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

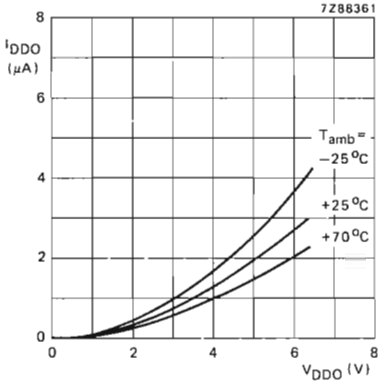


Fig. 11 Standby supply current as a function of standby supply voltage.

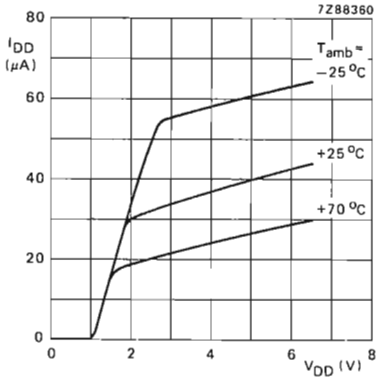


Fig. 12 Operating supply current as a function of operating supply voltage.

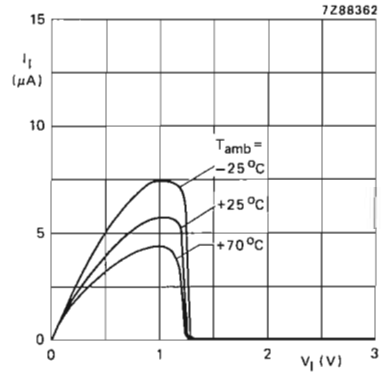


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

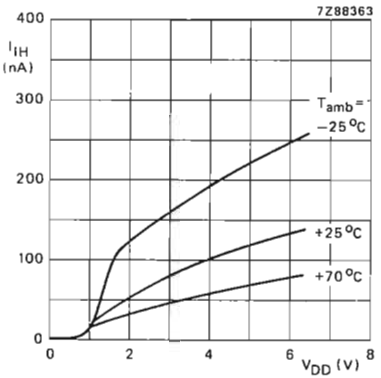


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

TYPICAL CURVES (continued)

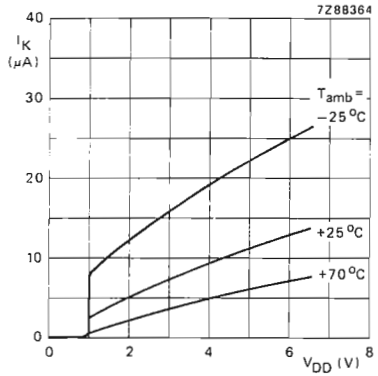


Fig. 15 Keyboard current as a function of supply voltage; X-pins connected to Y-pins.

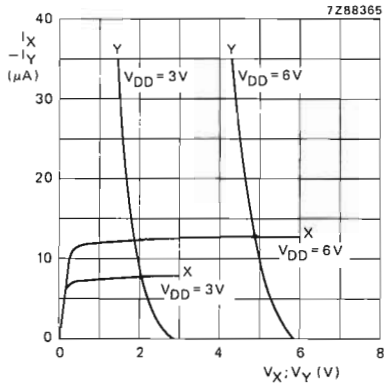


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

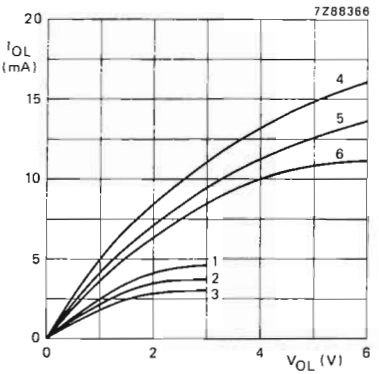


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

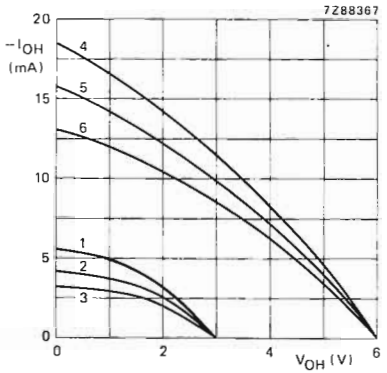
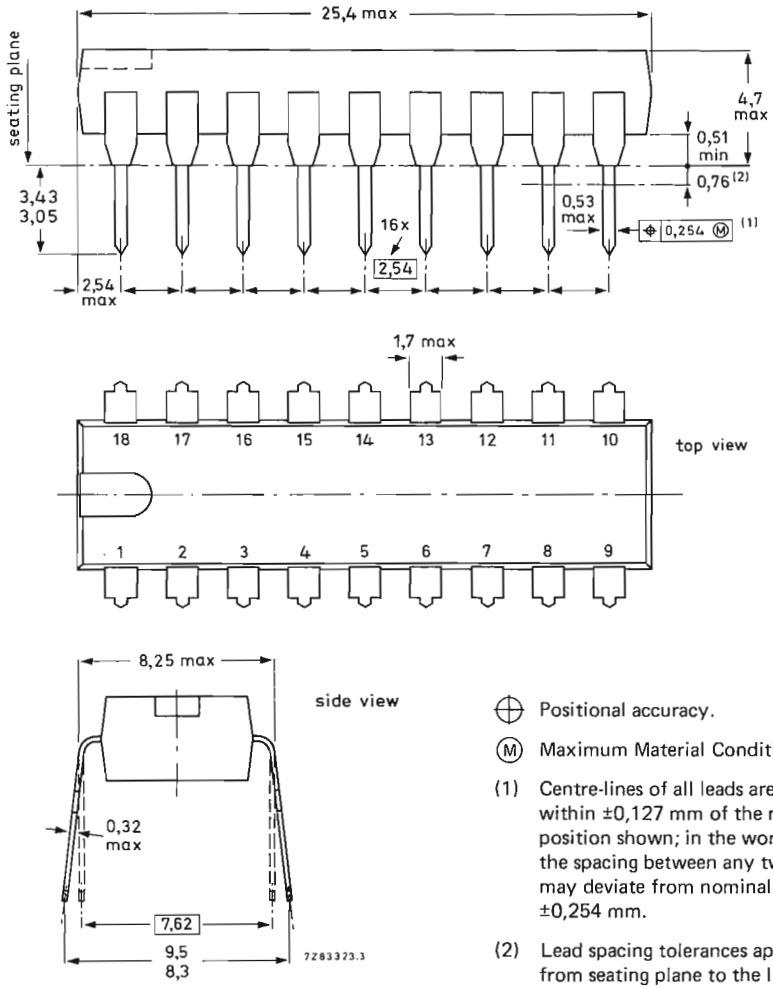


Fig. 18 Output (P-channel) source characteristics for M1 and DP.

Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102G)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

See next page.

SOLDERING

1. **By hand**

   Apply the soldering iron below the seating plane (or not more than 2 mm above it).
   If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

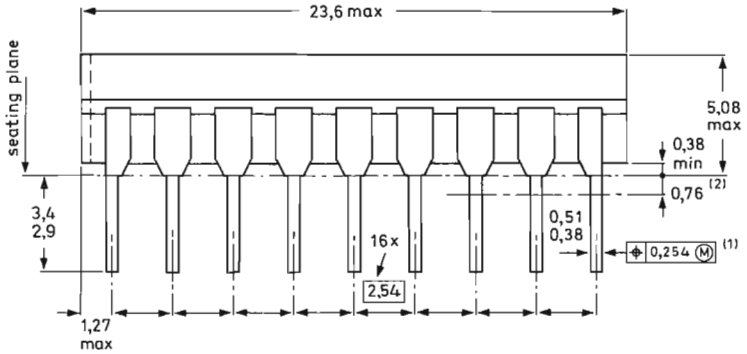
2. **By dip or wave**

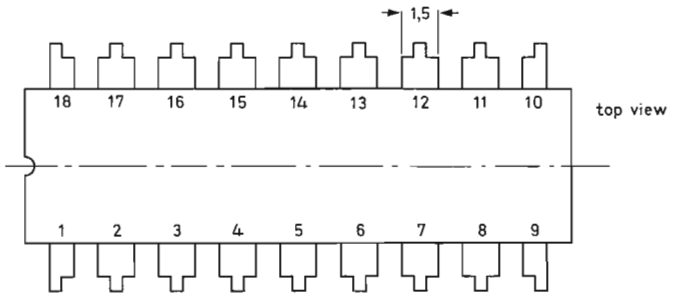
   The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

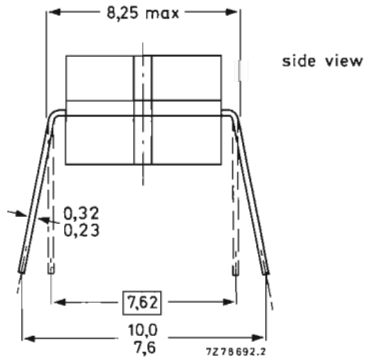
3. **Repairing soldered joints**

   The same precautions and limits apply as in (1) above.

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-133)







⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

C-MOS INTERRUPTED CURRENT-LOOP DIALLING CIRCUIT

The PCD3325 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The PCD3325 can regenerate access pauses during redial. During the original entry, access pauses are stored via the keyboard. A regenerated access pause can be terminated during redial in two ways: via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems. The PCD3325 is pin to pin compatible with the DF320 and the MT4320 (however, including additional functions).

The circuit has the following features:

- Operation from 2,5 V to 6 V supply.
- Static standby operation down to 1,8 V.
- Low current consumption; typ. 40 μA.
- Low static standby current; typ. 1 μA.
- On-chip oscillator for 3,58 MHz crystal.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz, 16 Hz and 20 Hz.
- Test pulse frequency: 932 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; > 160 ms (10 Hz dialling pulse frequency).
- Access pause generation automatically or via the keyboard.
- Access pause reset:
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINE

PCD3325P: 18-lead DIL; plastic (SOT-102G).

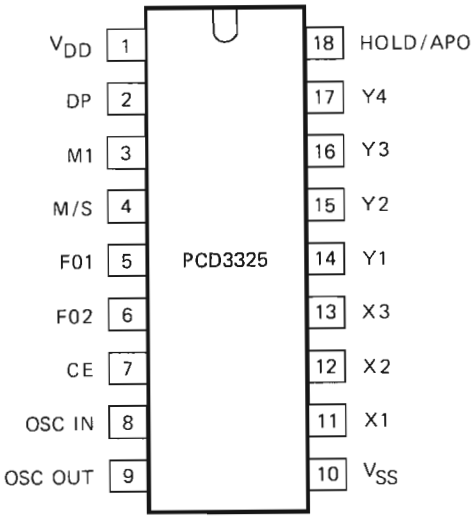


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
5	F01	the dialling pulse frequency is defined by the logic state of these two inputs
6	F02	
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	X1	column keyboard inputs with pull-down on chip
12	X2	
13	X3	
14	Y1	row keyboard inputs with pull-up on chip
15	Y2	
16	Y3	
17	Y4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

8	OSC IN	input and output of the on-chip oscillator
9	OSC OUT	

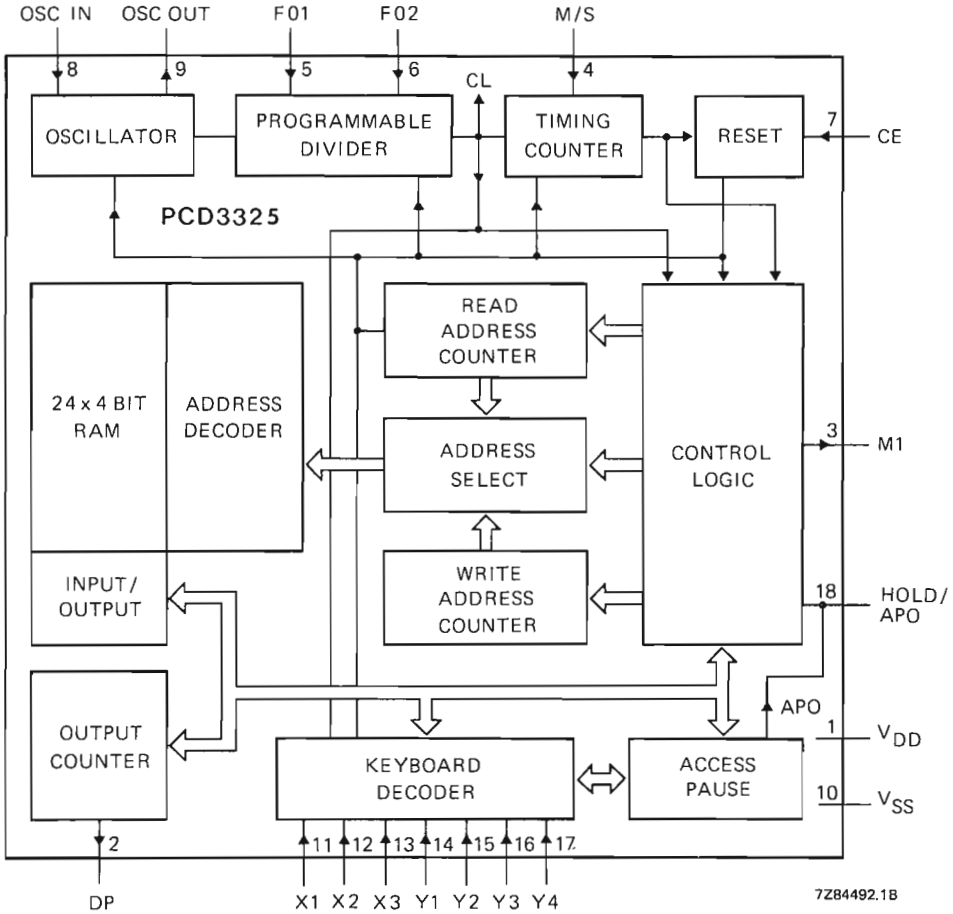


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (OSC IN, OSC OUT)

The time base for the PCD3325 is a crystal controlled on-chip oscillator which is completed only by connecting a crystal between the OSC IN and OSC OUT pins. The oscillator is followed by a frequency divider of which the division ratio can be externally set (F01 and F02) to provide one of four chip system clocks; three 'normal' clock frequencies and one higher test frequency.

Alternatively, the OSC IN input may be driven from an external clock signal.

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

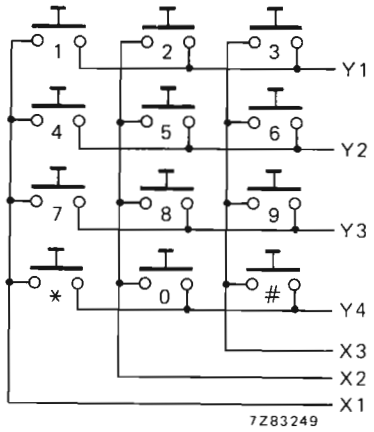
Debouncing keyboard entries

The column keyboard inputs to the integrated circuit (X_n) and the row keyboard inputs (Y_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig. 3, or to a double contact keyboard with a common left open (see Fig. 4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input or, when one column input is set HIGH and one row input is set LOW. Any other input combinations will be judged to be not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig. 5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the PCD3325. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

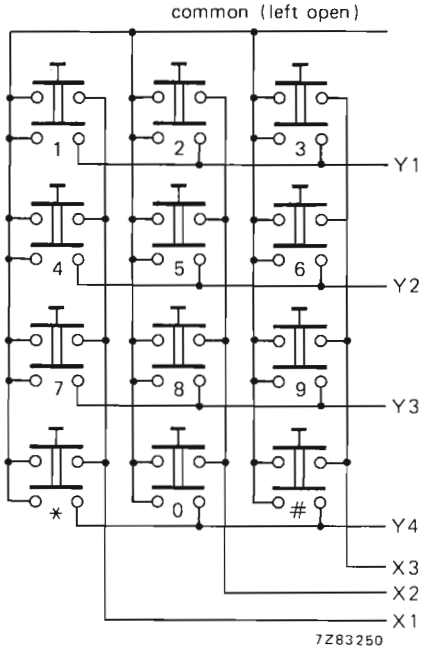


Fig. 4 Double contact keyboard.

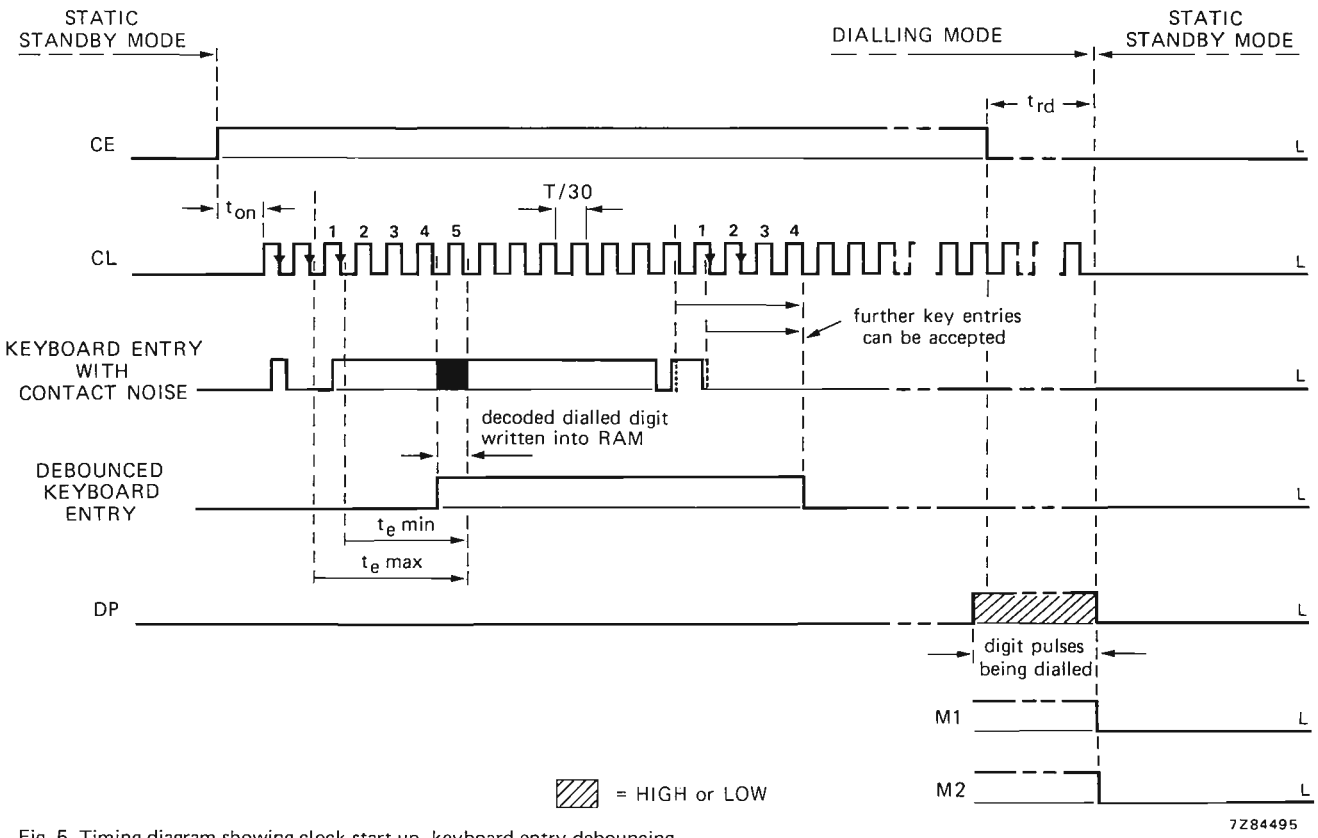


Fig. 5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.
N.B.: CL and M2 are internal signals.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 6.

Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and, ten clock pulse periods (t_d) later, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 6. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,8 V.

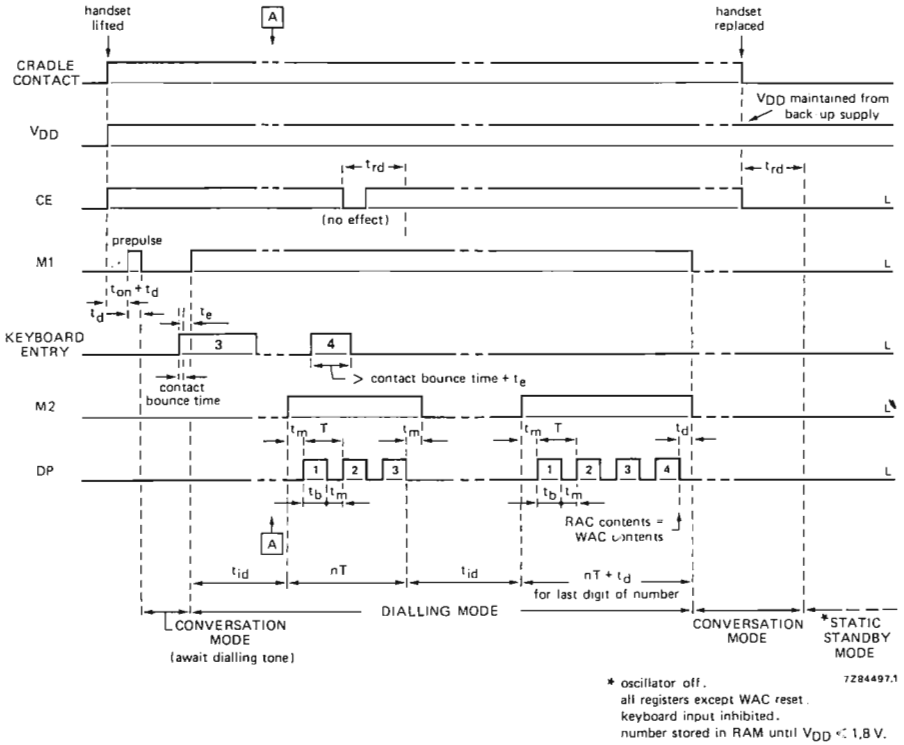


Fig. 6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

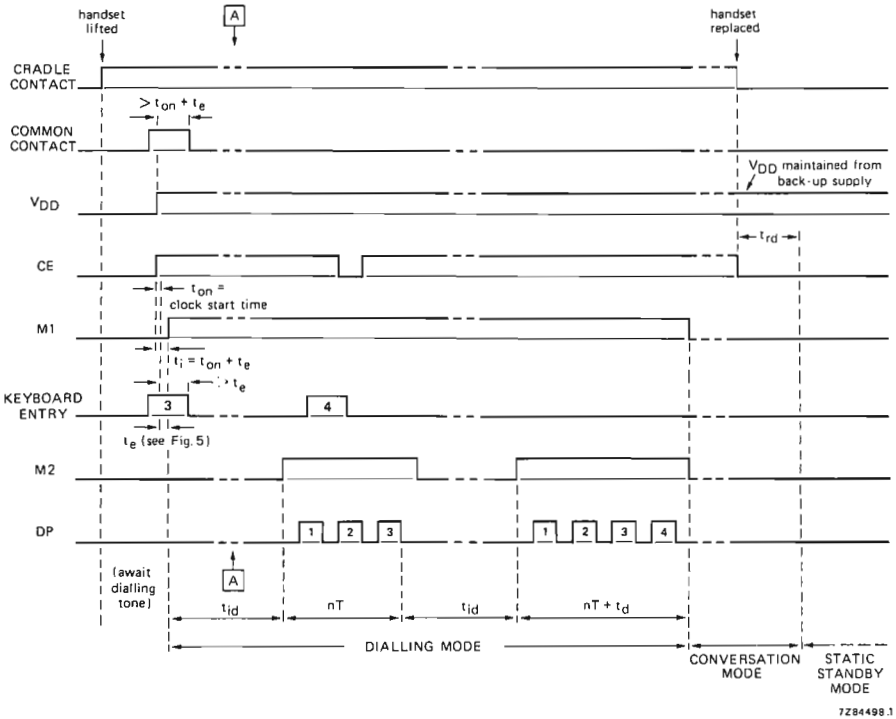


Fig. 7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 6 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

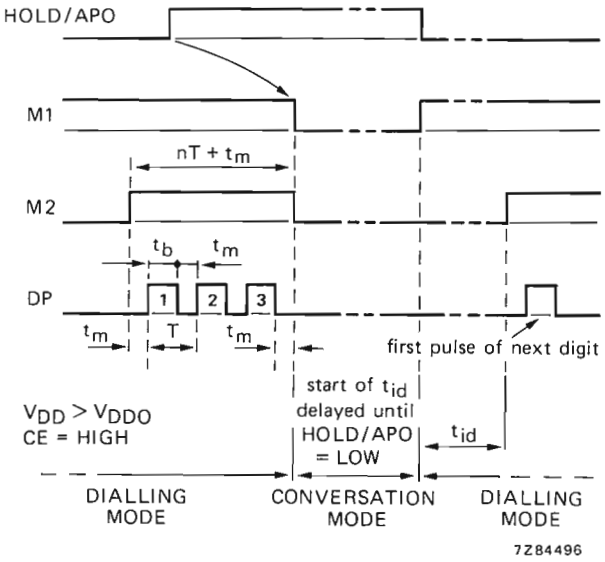


Fig. 8 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

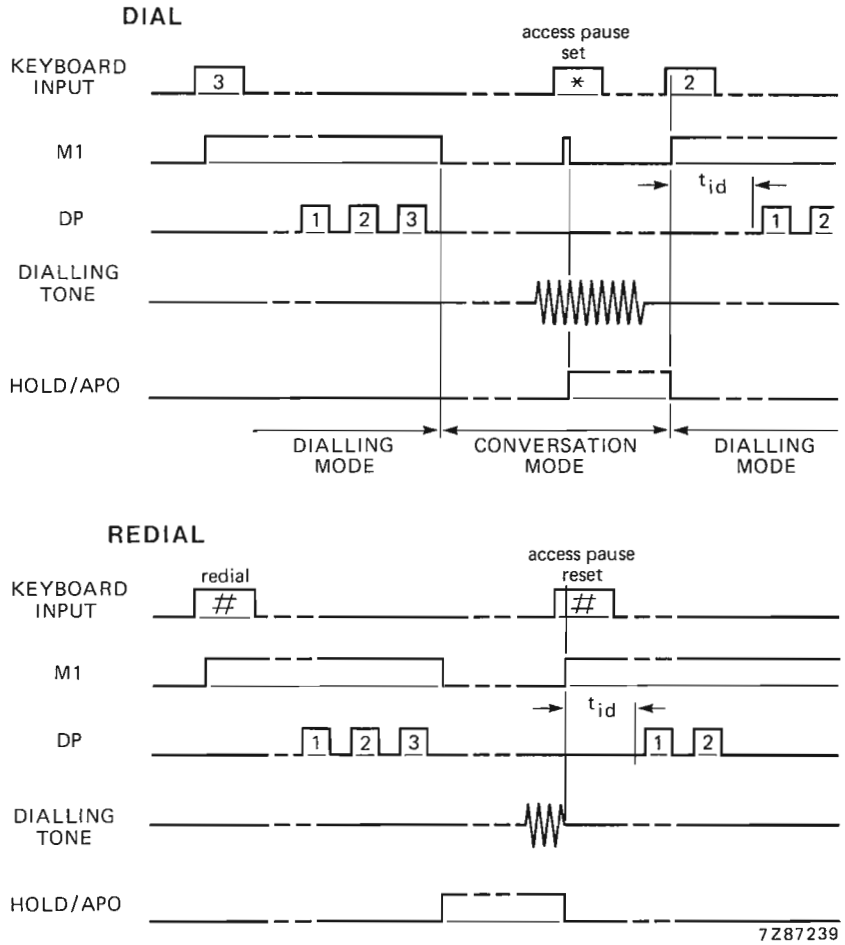


Fig. 9 Dialling sequence showing how an access pause code is stored in the RAM (DIAL) and how the access pause code is reset during the REDIAL.

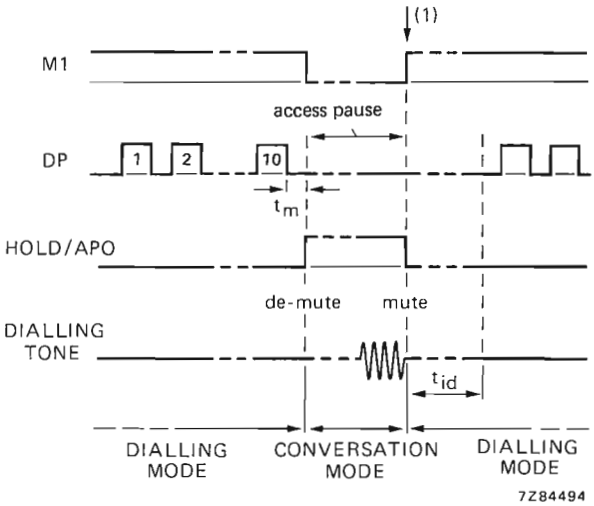
Note: access pause can be reset by pressing any key.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO) will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is stored in the RAM during original entry by pressing the access pause key (*) between entering the trunk exchange code and the subscriber code, or at any other moment an access pause is required. The number of access pauses that can be inserted in this manner is only limited by the capacity of the RAM (digits + access pauses $\leqslant 23$).

During redial, access pauses will be automatically regenerated.
Two methods of terminating an access pause:

1. Manually, by pressing the redial key (#)
2. With an external tone recogniser, by forcing HOLD/APO to LOW.



(1) a. Access pause reset by pressing redial key (#).
b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW.

Fig. 10 Timing diagram showing Access Pause Reset, during redial.

Note: access pause can be reset by pressing any key.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,58 MHz, R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified.

	symbol	min.	typ.	max.		conditions
Operating supply voltage	V_{DD}	2,5	3	6	V	
Standby supply voltage (note 1)	V_{DDO}	1,8	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	40	–	μA	CE = HIGH; notes 2, 3
	I_{DD}	–	50	100	μA	CE = HIGH; V_{DD} = 6 V; notes 2, 3
Standby supply current	I_{DDO}	–	1	5	μA	CE = LOW; note 2
	I_{DDO}	–	–	2	μA	V_{DD} = 1,8 V; T_{amb} = −25 to +70 °C
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = LOW
HIGH	I_{IH}	–	–	50	nA	CE = HIGH
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F01, F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	10	–	μA	X connected to Y, CE = HIGH
Keyboard 'ON' resistance	R_{KON}	–	–	500	Ω	contact ON; note 4
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 4
Other keyboard operation						
Input current for X_n 'ON'	I_{IH}	–	–	30	μA	V_I = 1,5 to 3 V
Input current for Y_n 'ON'	$-I_{IL}$	10	–	–	μA	V_I = 0 to 2,5 V
Input current Y_n	$-I_I$	–	–	0,7	mA	V_I = V_{SS}

Notes

1. V_{DDO} = 1,8 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between pins 8 and 9 < 3 pF.
4. Guarantees correct keyboard operation.

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.		conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	1,5	3,2	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,3	2,7	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
sink current	I_{OL}	50	130	300	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	45	110	250	μA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 3,579545 MHz

input levels of F01 and F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F01}	LOW	HIGH	LOW	HIGH		conditions (note 4)
		V_{F02}	LOW	HIGH	HIGH	LOW (test mode)		
		symbol						
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10,13	15,54	19,42	939,2	Hz	note 1
Dialling pulse period	$1/f_{DP}$	T_{DP}	98,7	64,4	51,5	1,073	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	303,9	466,1	582,6	27965	Hz	
Break time (note 2)	$3/5 \times T_{DP}$	t_b	59,2	38,6	30,9	0,644	ms	M/S = H; n.c.
Make time (note 2)	$2/5 \times T_{DP}$	t_m	39,5	25,8	20,6	0,429	ms	M/S = H; n.c.
Break time (note 3)	$2/3 \times T_{DP}$	t_b	65,8	42,9	34,6	0,715	ms	M/S = L
Make time (note 3)	$1/3 \times T_{DP}$	t_m	32,9	21,5	17,2	0,358	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	790	515	412	8,58	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	158	103	82,4	1,72	ms	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33	21,5	17,2	0,358	ms	
Debounce time								
min	$4/30 \times T_{DP}$	$t_{e\,min}$	13,2	8,58	6,87	0,143	ms	
max.	$1/6 \times T_{DP}$	$t_{e\,max}$	16,5	10,7	8,58	0,179	ms	
Clock start-up time		$t_{on\,typ}$	4	—	—	—	ms	CE: $V_{SS} \rightarrow V_{DD}$ (note 5)
Initial data entry time (typ.)	$t_{on} + t_e$	t_i	18	14	12	4	ms	

Notes

1. Exactly 10 Hz with 3,5328 MHz crystal.
2. Mark-to-space ratio: 3:2.
3. Mark-to-space ratio: 2:1.
4. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.
5. Stray capacitance between pins 8 and 9: < 3 pF.

TYPICAL CURVES

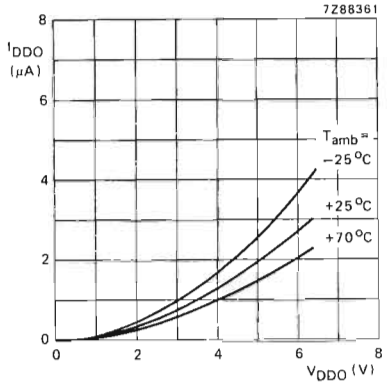


Fig. 11 Standby supply current as a function of standby supply voltage.

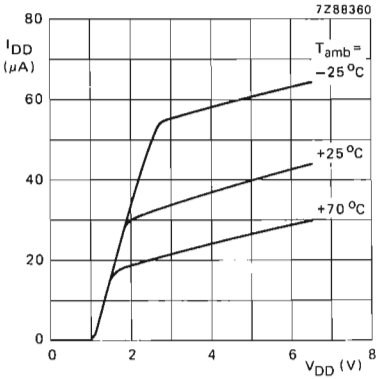


Fig. 12 Operating supply current as a function of operating supply voltage.

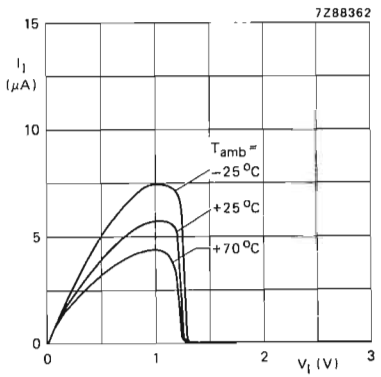


Fig. 13 Pull-down input current as a function of input voltage at V_{DD} = 3 V.

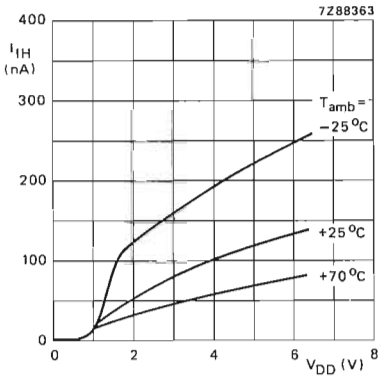


Fig. 14 Pull-down input current as a function of supply voltage at $V_I = V_{DD}$.

DEVELOPMENT SAMPLE DATA

TYPICAL CURVES (continued)

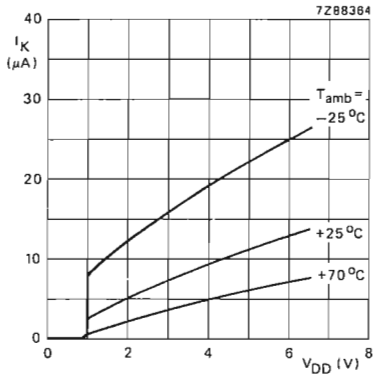


Fig. 15 Keyboard current as a function of supply voltage;
X-pins connected to Y-pins.

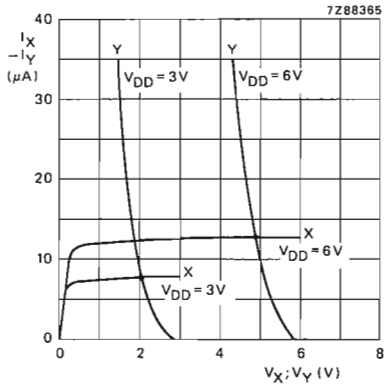


Fig. 16 Keyboard input characteristics at T_{amb} = 25 °C.

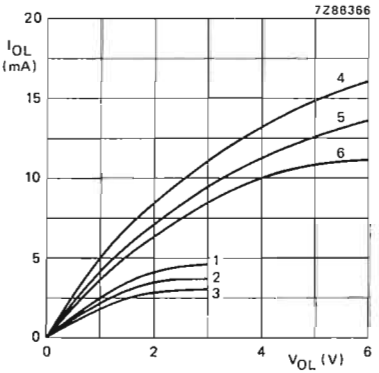


Fig. 17 Output (N-channel) sink characteristics for M1 and DP.

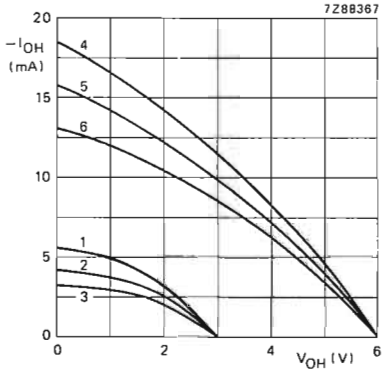
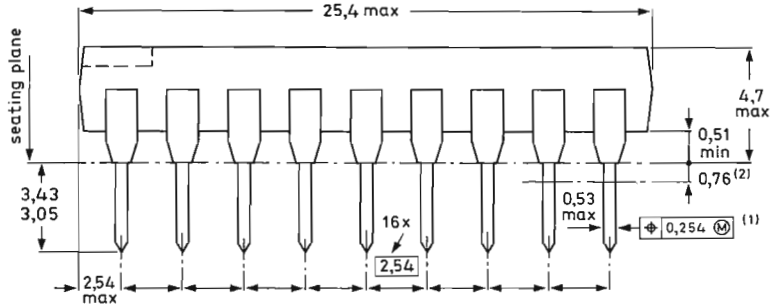


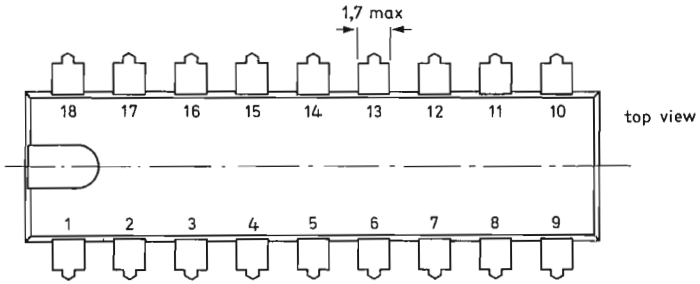
Fig. 18 Output (P-channel) source characteristics for M1 and DP.

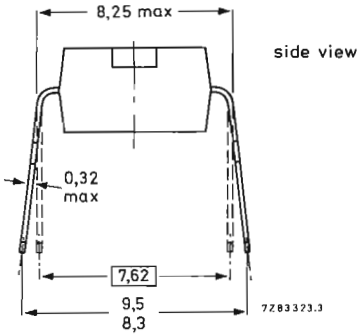
Curves for Figs 17 and 18

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	1	4
+25 °C	2	5
+70 °C	3	6

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102G)







⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

See next page.

DEVELOPMENT SAMPLE DATA

SOLDERING

1. **By hand**

   Apply the soldering iron below the seating plane (or not more than 2 mm above it).
   If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. **By dip or wave**

   The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. **Repairing soldered joints**

   The same precautions and limits apply as in (1) above.

Pulse repertory dialler/telephone-set controller

PULSE REPERTORY DIALLER/TELEPHONE-SET CONTROLLER

The PCD3341 is a ROM version of the PD3340 microcomputer. The latter has been adapted for telephony from the PCF8500 family. Based on an 8-bit CPU, 224 byte RAM and 2kbyte ROM (mask programmable), the PCD3341 can convert keyboard input data into pulses suitable for loop disconnect dialling, and can control display and repertory functions and dual-tone multi-frequency (DTMF) dialling in 'extended feature' telephones. The PCD3341 has the PFC8500 instruction set (8048 instruction set with minor modifications).

Features

- pulse dialling
- redial
- extended redial
- direct dialling (emergency call)
- on-chip 10 repertory call numbers, each 16 digits long
- access pause generation by recognition of first digit(s)
- facility to add digits after redial or repertory dialling
- standard 4 x 4 keyboard function keys
- keyboard expansion
- extension for: DTMF dialling, repertory dialling (up to 100 numbers), liquid-crystal display via serial I/O bus (I²C bus)
- on-chip oscillator for 3,58 MHz crystal
- facility for driving external oscillator

QUICK REFERENCE DATA

Supply voltage	2,5 V to 6 V
Static standby operation	
without reset	down to 1,8 V
with reset	down to 1,0 V
Low current consumption	
dialling mode	typ. 300 μA
conversation mode	typ. 150 μA
standby mode	typ. 2 μA

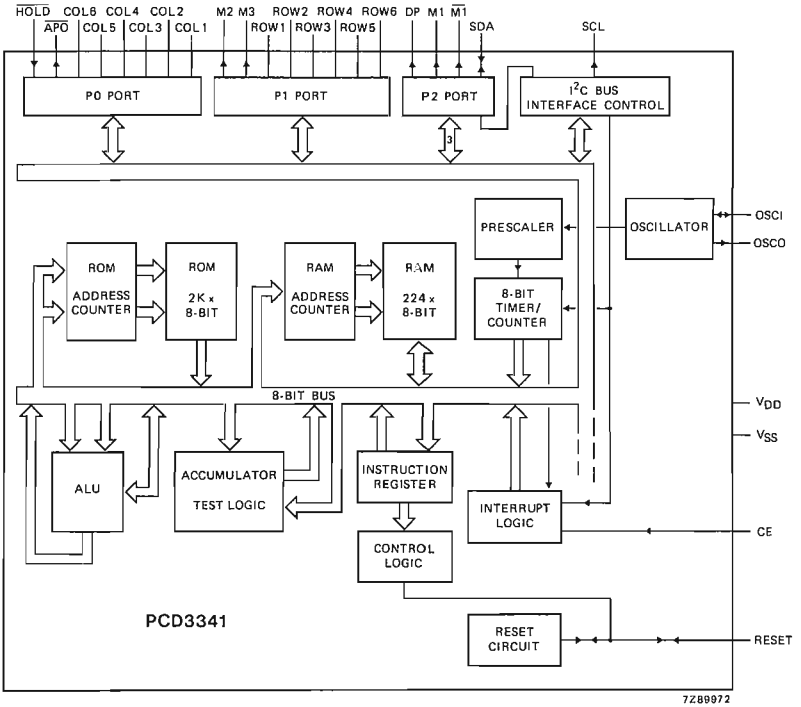
Encapsulation: SOT-117D (28 pin DIL, plastic)
SO-28/SOT-136A (28 pin flat-pack)

DESCRIPTION

PCD 3340

- 8-bit CPU structure
- 2 kbyte ROM
- 224 byte RAM
- 20 quasi-directional port pins (2 x 8 + 1 x 4)
- serial input/output port (I^2C bus)
- mask-programmable push-pull on all ports
- individual set/reset option on all ports
- internal power on reset circuit
- timer/event counter
- interrupt input (CE)

BLOCK DIAGRAM



Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

Microcomputer peripherals (DTMF/MODEM, RAM, LCD, clock)

DTMF/MODEM GENERATOR

The PCD3311 is intended to provide the DTMF combinations required for tone dialling systems in telephone sets where the control functions are performed by a microcomputer. The device can interface directly with all standard microcomputers, accepting both 6-bit parallel input and serial data input (I^2C bus). It uses a 3,58 MHz quartz crystal or a clock of the same frequency provided by the microcomputer. The device can also provide the MODEM frequencies according to CCITT (V21/23) and USA (B103/202) specifications.

Features

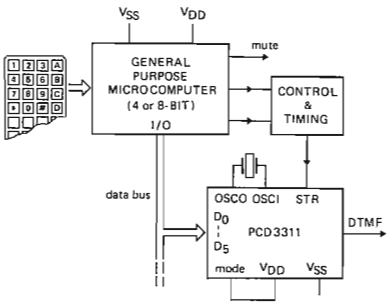
- stabilised output level
- low distortion by on-chip filtering (CEPT CS203 compatible)
- latched inputs for data-bus applications
- mode select input (parallel or serial data input)
- strobe input (data loaded in parallel mode)
- MODEM frequency generator
- single frequency generator

QUICK REFERENCE DATA

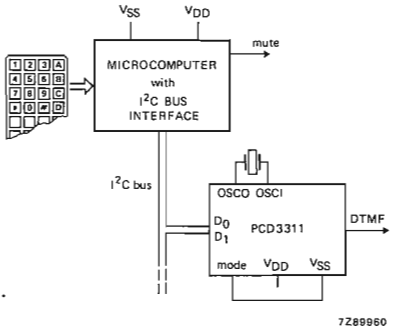
Operating supply voltage	typ. 3 V
Current consumption	
in operating mode	typ. 0,5 mA
in standby mode (oscillator on)	max. 200 μA
in standby mode (oscillator off)	max. 10 μA
Frequency accuracy	0,6%
Low-frequency level	typ. 153 mV
Pre-emphasis	(2,1 ± 0,7) dB
Start-up time	typ. 4 ms

Encapsulation: SOT-27 (14-pin DIL plastic)

Application information



PCD3311 driven by a microcomputer with parallel data-bus



PCD3311 driven by a microcomputer with serial data-bus

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DTMF/MODEM GENERATOR

The PCD3312 is intended to provide the DTMF combinations required for tone dialling systems in telephone sets where the control functions are performed by a microcomputer with I²C interface. The device can interface directly with the serial bus. It uses a 3,58 MHz quartz crystal or a clock of the same frequency provided by the microcomputer. The device can also provide the MODEM frequencies according to CCITT (V21/23) and USA (B103/202) specifications.

Features

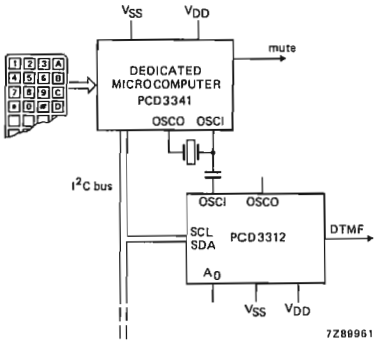
- stabilized output level
- low distortion by on-chip filtering (CEPT CS203 compatible)
- I²C bus compatible
- MODEM frequency generator
- single frequency generator

QUICK REFERENCE DATA

Operating supply voltage	typ. 3 V
Current consumption	
in operating mode	typ. 0,5 mA
in standby mode (oscillator on)	max. 200 μA
in standby mode (oscillator off)	max. 10 μA
Frequency accuracy	0,6%
Low-frequency level	typ. 153 mV
Pre-emphasis	(2,1 ± 0,7) dB
Start-up time	typ. 4 ms

Encapsulation: SOT-97A (8 pin DIL plastic)

Application information



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

128 x 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD8571 is a low-power 1024-bit static CMOS/RAM, organized as 128 words of 8 bits each. Data and address are transferred serially via a two-line bidirectional bus (I²C). Automatic word address incrementing in read/write modes minimizes bus traffic. Three hardware address pins A0, A1 and A2 identify when several devices are connected on the bus, which allows the use of up to 8 RAMs without additional hardware (see Fig. 13).

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 5 μA
- Power down mode typ. 50 nA
- Low power consumption
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3330 applications)
- Radio and television — channel presets
- Video cassette recorder
- General purpose — RAM expansion for the microcomputer families MAB8400 and PCF8500

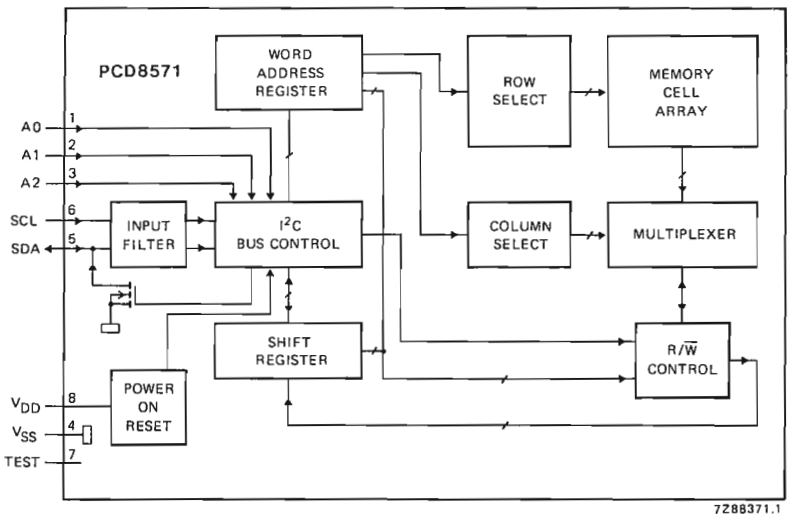


Fig. 1 Block diagram.

PACKAGE OUTLINES

8-lead DIL; plastic (SOT-97A).

PINNING

1 to 3	A0 to A2	address inputs	
4	V_{SS}	negative supply	
5	SDA	serial data line	I²C bus
6	SCL	serial clock line	
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power down mode, see Fig. 14 and 15)	
8	V_{DD}	positive supply	

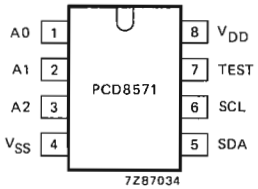


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 8 V
Input voltage range (any pin)	V_I	V_{SS}−0,8 to V_{DD} + 0,8 V*
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature range	T_{amb}	−25 to + 70 °C

* Impedance min. 500 Ω.

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0; T_{amb} = −25 to + 70 °C, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	3	6	V
Supply current					
at V_{DD} = 5 V; f_{SCL} = 100 kHz					
operating	I_{DD}	–	50	200	μA
standby	I_{DDO}	–	–	5	μA
Power-on reset voltage level *					
at V_{SCL} = V_{SDA} = V_{DD}	V_{REF}	1,5	1,9	2,3	V
Input SCL; input/output SDA					
Input voltage LOW	V_{IL}	–	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	–	V
Output current LOW					
V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH					
at V_{OH} = V_{DD}	I_{OH}	–	–	100	nA
Input leakage current (A0, A1, A2)					
V_{IN} = V_{DD} or V_{SS}	$\pm I_{IN}$	–	–	100	nA
Clock frequency (see Fig. 7)	f_{SCL}	0	–	120	kHz
Input capacitance (SCL, SDA)					
at V_I = V_{SS}	C_I	–	–	7	pF
Noise suppression time constant					
at SCL and SDA input	T_I	0,25	1,0	2,5	μs
LOW V_{DD} data retention characteristics					
Supply voltage for data retention	V_{DR}	1	1,2	–	V
Data retention current					
at V_{DR} = 1,0 V	I_{DR}	–	–	2	μA
Power down mode (see Fig. 14)					
at T_{amb} = 25 °C	I_{PD}	–	50	–	nA

* The power-on reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for two-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

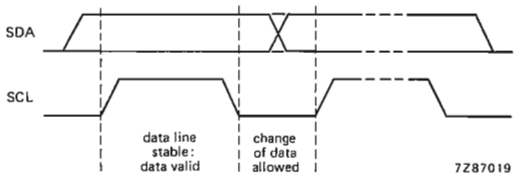


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

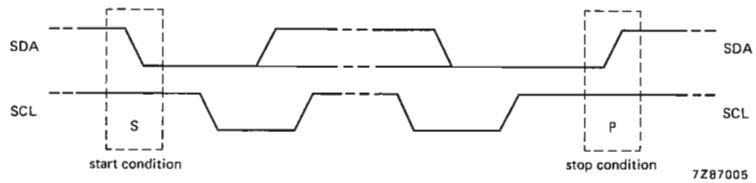


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

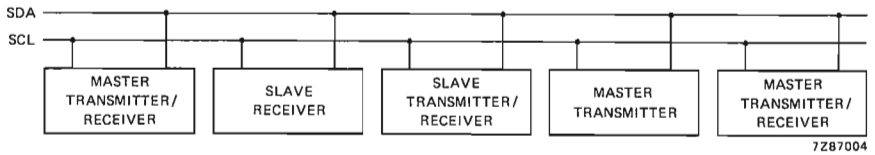


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

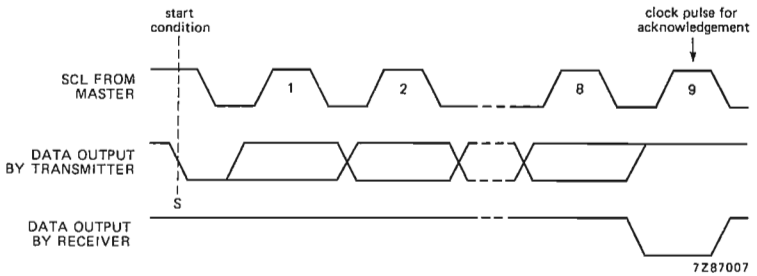


Fig. 6 Acknowledgement on the I^2C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCD8571 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

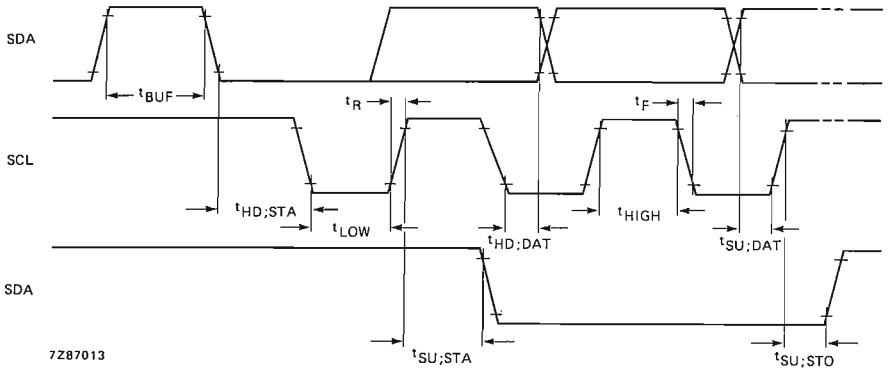


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values referred to V_{IH} and V_{IL} levels.

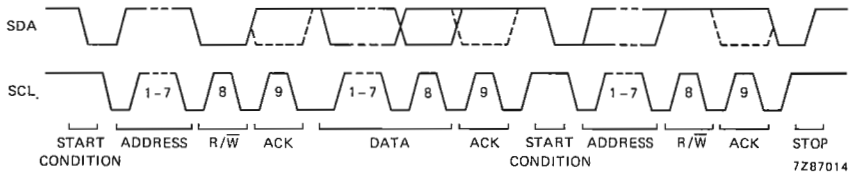


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

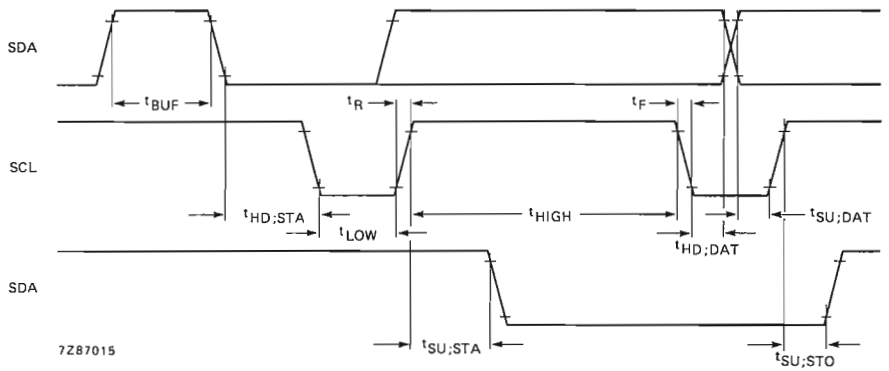


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the values referred to V_{IH} and V_{IL} levels, for definitions see high-speed mode.

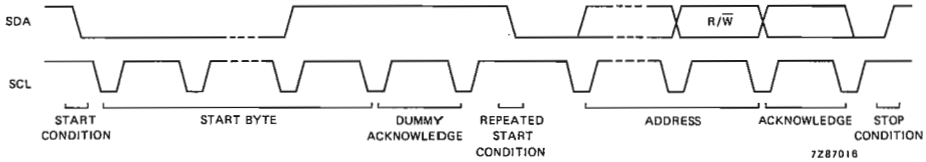


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Addressing

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCD8571 READ and WRITE cycles is shown in Fig. 11.

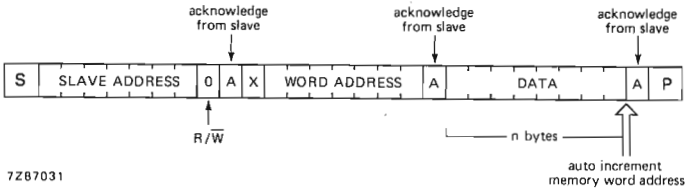


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

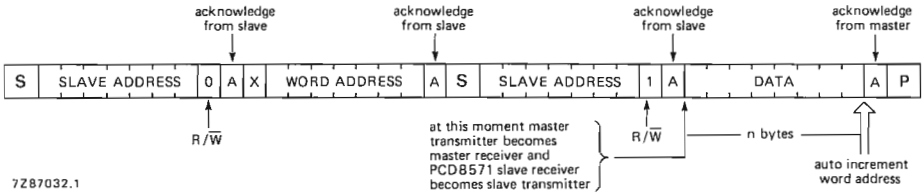


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

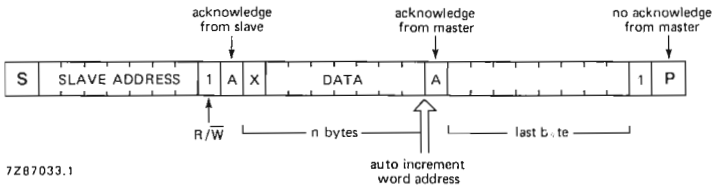


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

Note

X = don't care bit.

APPLICATION INFORMATION

The PCD8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

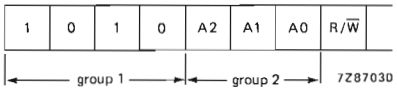


Fig. 12 PCD8571 address.

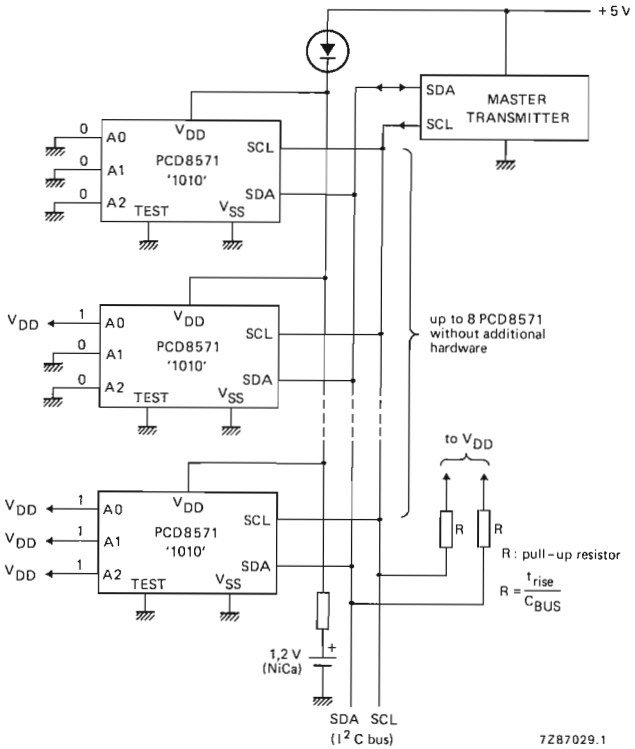


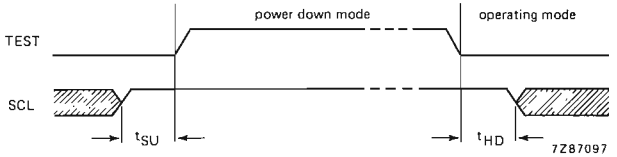
Fig. 13 PCD8571 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER DOWN MODE

With the condition TEST = A2 = A1 = A0 = V_{DD} the PCD8571 goes into the power down mode.



Where:
$t_{SU} \geq 4\ \mu s$
$t_{HD} \geq 4\ \mu s$

Fig. 14 Timing for power down mode.

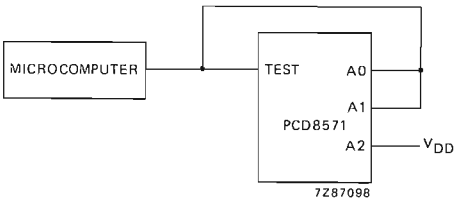
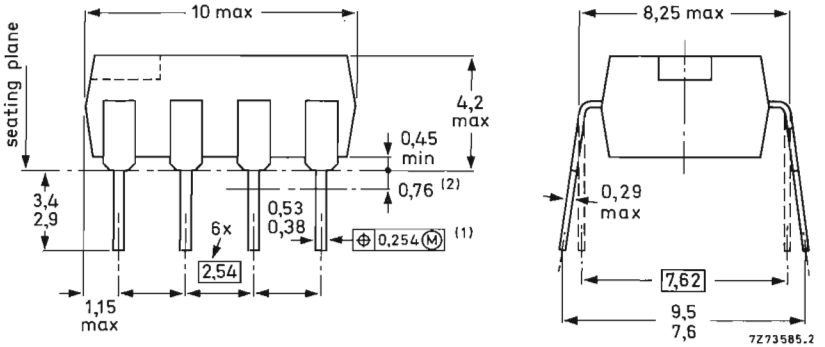


Fig. 15 Application for power down mode.

Note

1. In the operating mode TEST = 0 (A0 = A1 = 0; A2 = 1).
2. In the power down mode TEST = A0 = A1 = A2 = 1.

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCB8573 is a low threshold, monolithic CMOS circuit that functions as a real time clock/calendar in the Inter IC (I^2C) bus-orientated microcomputer systems. The device includes an addressable time counter and an addressable alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two line bidirectional bus (I^2C). To transfer data a second supply voltage must be present. Back-up for the clock during supply interruptions is provided by a 1,2 V nickel cadium battery. The time base is generated from a 32,768 kHz crystal-controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

Supply voltage range (logic)	$V_{DD}-V_{SS1}$	1,1 to 2,6	V
Supply voltage range (level shifter)	$V_{DD}-V_{SS2}$	2,5 to 6,0	V
Crystal oscillator frequency	f_{osc}	typ. 32 768	Hz

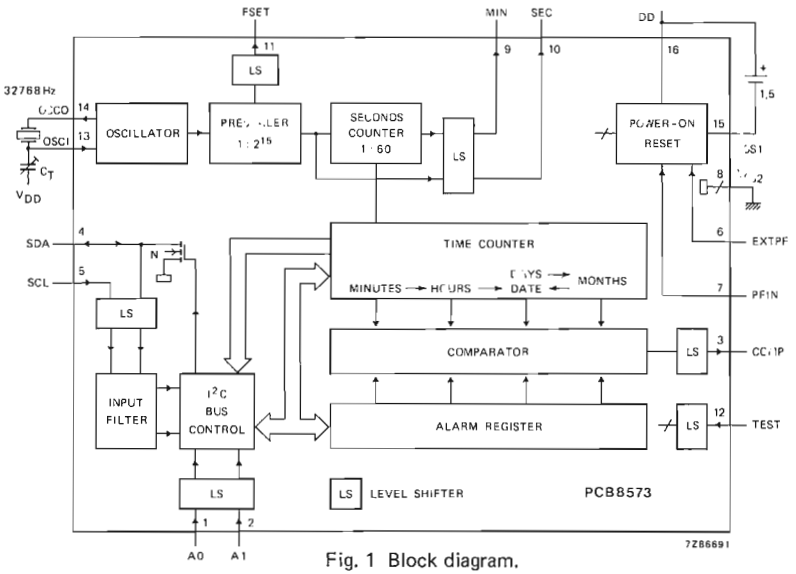


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

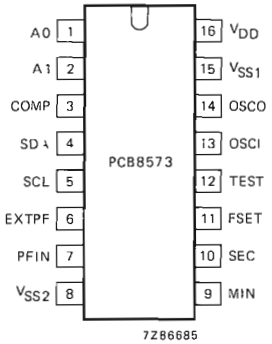


Fig. 2 Pinning diagram.

PINNING

1	A0	level shifter input	
2	A1	level shifter input	
3	COMP	comparator output	
4	SDA	serial data line*	I²C bus
5	SCL	serial clock line	I²C bus
6	EXTPF	external power fail flag input	
7	PFIN	internal power fail flag input	
8	V_{SS2}	negative supply 2	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator set output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

The following is a functional description of the PCB8573.

Oscillator

The PCB8573 has an intergrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer (C_T) is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I²C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

* Output open drain n-channel.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (see note)
			or 29 → 01	
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note: Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. The effect of both COMP and POWF being set is dependent upon the master software. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal, for application with $V_{DD}-V_{SS1} > V_{TH1}$, or by an externally generated power fail signal, for application with $V_{DD}-V_{SS1} < V_{TH1}$. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internal or external controlled POWF can be selected by input EXTPF as shown in Table 2.

FUNCTIONAL DESCRIPTION (continued)

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internal
0	1	test mode
1	0	power fail is sensed external
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip, when the supply voltage $V_{DD}-V_{SS2}$ is 1,5 V $\leq (V_{DD}-V_{SS1}) \leq$ 2,5 V.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcomputer to the internal $\geq$ 1,1 V supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common mode of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supply. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages, for applications the source capability on these outputs is cut off when the supply voltage V $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for two-way, 2 line-communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line ate this time will be interpreted as control signals.

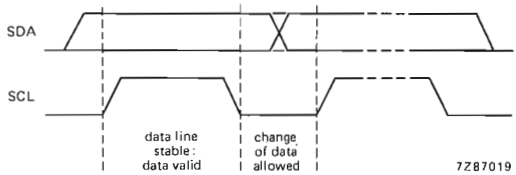


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

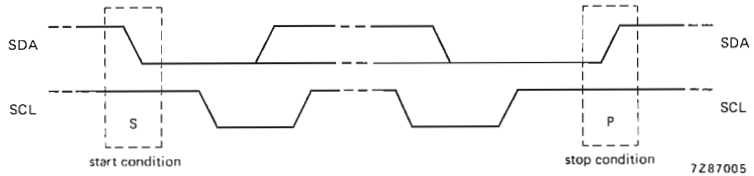


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

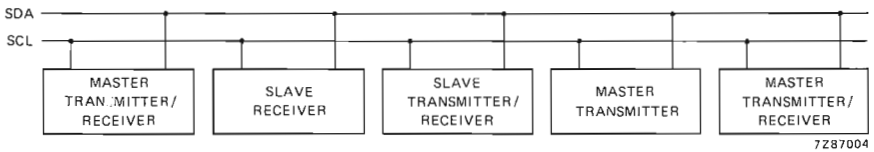


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 13 and Fig. 14.)

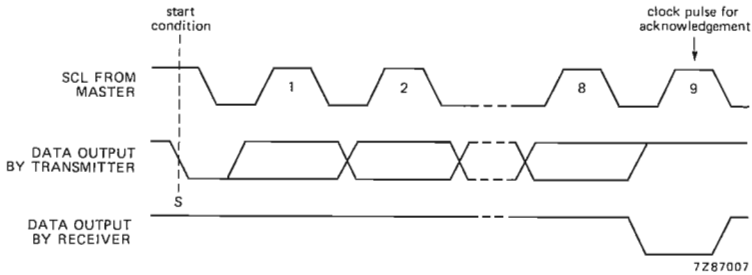


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCB8573 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

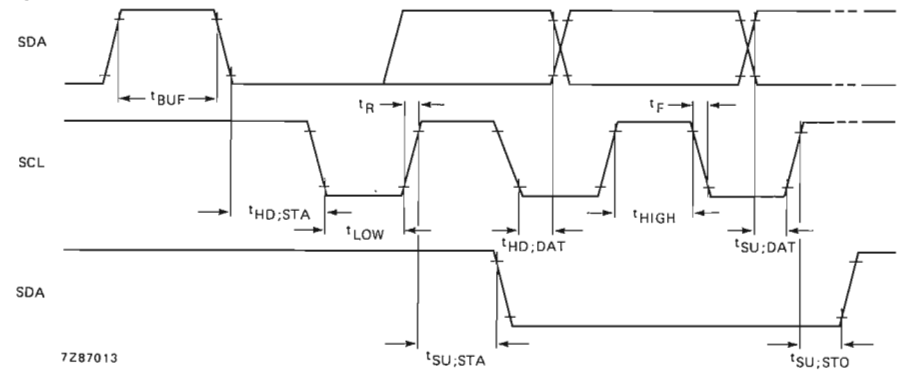


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geq t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geq 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geq 250$ ns	Data set-up time
t_R	$t \leq 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leq 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geq t_{LOWmin}$	Stop condition set-up time

Note

All the values referred to V_{IH} and V_{IL} levels.

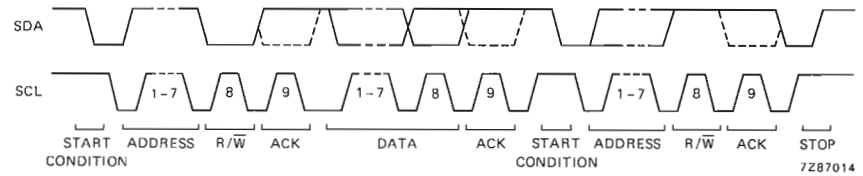


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

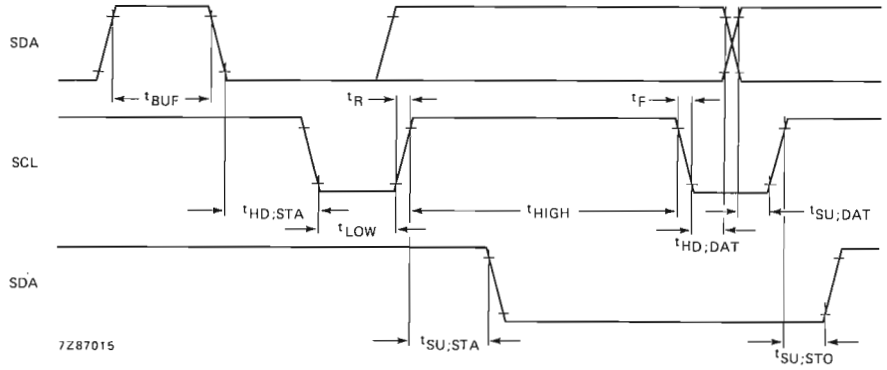


Fig. 9 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geq 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geq 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geq 0\ \mu s$
$t_{SU;DAT}$	$t \geq 250$ ns
t_R	$t \leq 1\ \mu s$
t_F	$t \leq 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the values referred to V_{IH} and V_{IL} levels, for definitions see high-speed mode.

* Only valid for repeated start code.

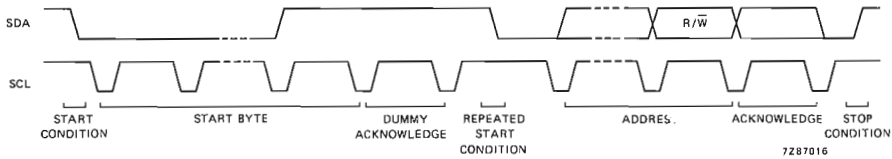


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 11.

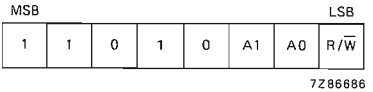


Fig. 11 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 12 and Fig. 13.

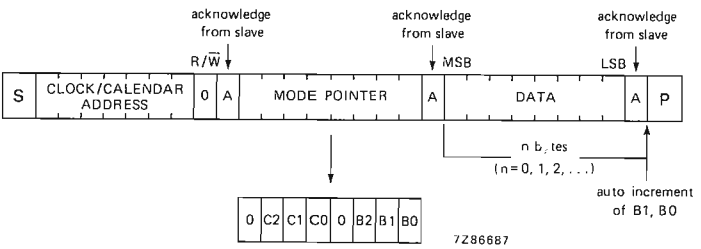


Fig. 12 Master transmitter transmits to clock/calendar slave receiver.

This mode is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. –30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

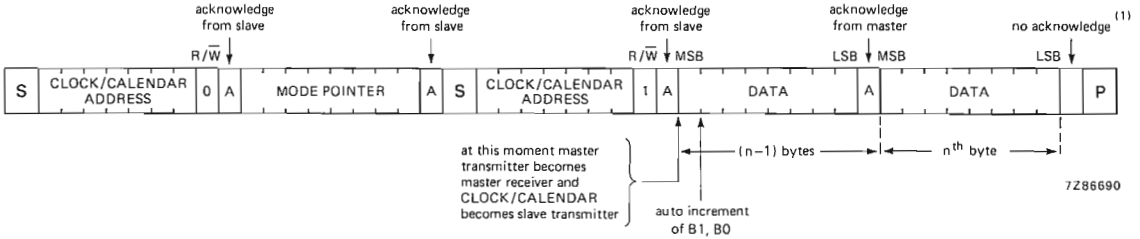
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where "X" is the don't care bit and "D" is the data bit.

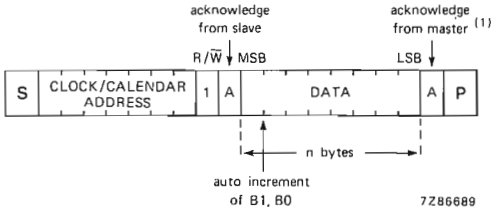
Acknowledgement response of the clock calendar as the slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 13 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 14 Master reads clock/calendar immediately after first bite.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where "X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where: "D" is the data bit.
* = minutes.
** = seconds.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges	$V_{DD}-V_{SS1}$		−0,3 to + 8 V
	$V_{DD}-V_{SS2}$		−0,3 to + 8 V
Voltage on pins 4 and 5			V_{SS2}−0,8 to V_{DD} + 0,8 V*
Voltage on pins 6, 7, 13 and 14			V_{SS1}−0,6 to V_{DD} + 0,6 V
Voltage on any other pin			V_{SS2}−0,6 to V_{DD} + 0,6 V
Input current	I_I	max.	100 μA
Output current	I_O	max.	10 mA
Power dissipation per output	P_O	max.	100 mW
Total power dissipation per package	P_{tot}	max.	200 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

* Impedance min. 500 Ω.

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = 0 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage level shifter	$V_{DD}-V_{SS2}$	2,5	5	6,0	V
Supply voltage logic	$V_{DD}-V_{SS1}$	1,1	–	2,6	V
Supply current V_{SS1} at $V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	–	10	μA
Supply current V_{SS2} at $V_{DD}-V_{SS2}$ = 5 V (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs					
Inputs SCL, SDA, A0, A1, TEST					
Input leakage current at $V_{DD}-V_{SS2}$ = 6 V; T_{amb} = 25 °C					
V_I = 6 V	I_I	–	–	1	μA
V_I = 0 V	$-I_I$	–	–	1	μA
Inputs SCL, SDA, A0, A1, TEST (level shifter inputs) at $V_{DD}-V_{SS2}$ = 2,5 to 6 V					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW	V_{IL}	–	–	0,3 x V_{DD}	V
Inputs EXTPF, PFIN at $V_{DD}-V_{SS1}$ = 1,1 to 2,6 V					
Input voltage HIGH	V_{IH}	0,7 x $V_{DD}-V_{SS1}$		–	V
Input voltage LOW	V_{IL}	–	–	0,3 x $V_{DD}-V_{SS1}$	V
Input leakage current at $V_{DD}-V_{SS1}$ = 2,6 V; T_{amb} = 25 °C					
$V_I = V_{DD}$	I_I	–	–	0,1	μA
$V_I = V_{SS1}$	$-I_I$	–	–	0,1	μA

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs					
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)					
Output voltage HIGH)					
at $V_{DD}-V_{SS2}$ = 2,5 V $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output voltage LOW					
at $V_{DD}-V_{SS2}$ = 2,5 V I_O = 0,3 mA	V_{OL}	–	–	0,4	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V I_O = 1,6 mA	V_{OL}	–	–	0,4	V
Output SDA (N-channel open drain)					
Output "ON": I_O = 3 mA at $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current)					
V_O = 6 V; T_{amb} = 25 °C at $V_{DD}-V_{SS2}$ = 6 V	I_O	–	–	1	μA
Internal threshold voltage					
Power failure detection	V_{TH1}	1	1,2	1,4	V
Power "ON" reset at $V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals					
Input EXTPF at $V_{DD}-V_{SS1}$ = 1,1 to 2,6 V	t_r, t_f	–	–	1	μs
Input PFIN at $V_{DD}-V_{SS1}$ = 1,1 to 2,6 V (10% to 90% ($V_{DD}-V_{SS1}$))	t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN at $V_{DD}-V_{SS2}$ = 2,5 to 6 V between V_{IL} and V_{IH} levels					
rise time	t_r	–	–	1	μs
fall time	t_f	–	–	0,3	μs

parameter	symbol	min.	typ.	max.	unit
Frequency at SCL					
at $V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (see Figs 7 and 9)	t_{LOW}	4,7	–	–	μs
Pulse width HIGH (see Figs 7 and 9)	t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA output	T_I	0,25	1	2,5	μs
Input capacitance (SCL, SDA)	C_I	–	–	7	pF
Oscillator					
Integrated oscillator capacitance	C_{out}	–	40	–	pF
Oscillator feedback resistance	R_f	–	3	–	MΩ
Oscillator stability for: $\Delta(V_{DD}-V_{SS1})$ = 100 mV at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	kΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	–	5,25	–	pF

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION

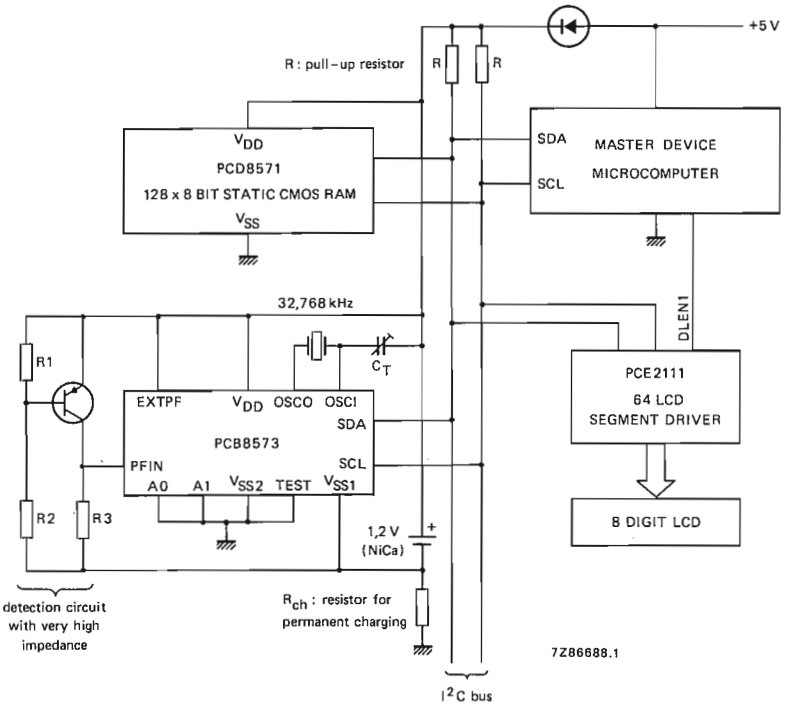
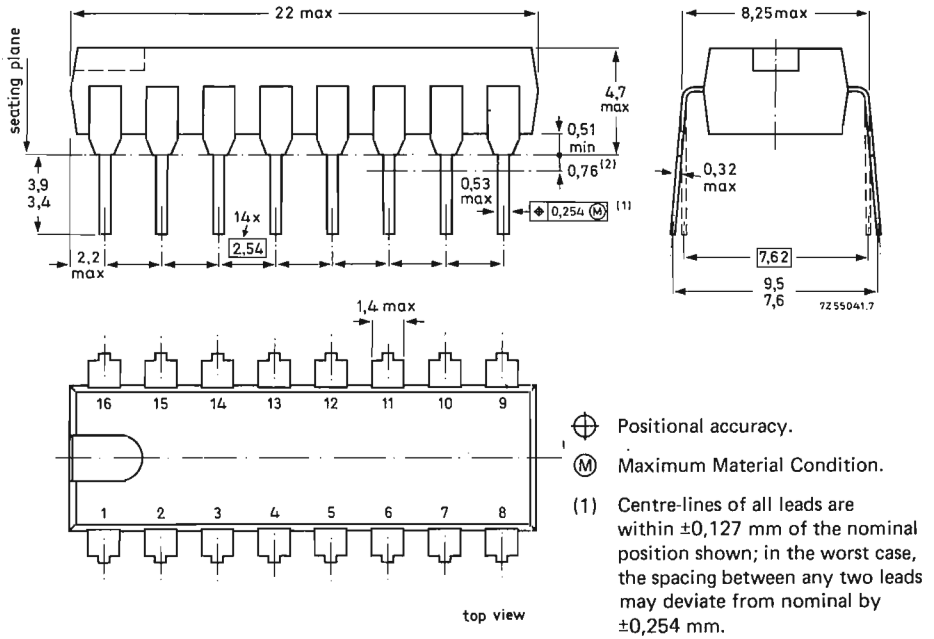


Fig. 15 Application example of the PCB8573 clock/calendar.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

DEVELOPMENT SAMPLE DATA

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

LCD DUPLEX DRIVER

GENERAL DESCRIPTION

The PCE2111 is a single chip, silicon gate C-MOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 64 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcomputers. All inputs are C-MOS/N-MOS compatible.

Features

- 64 LCD-segment drive capability.
- Supply voltage 2,25 to 6,5 V.
- Low current consumption.
- Serial data input.
- CBUS control.
- One-point built-in oscillator.
- Expansion possibility.

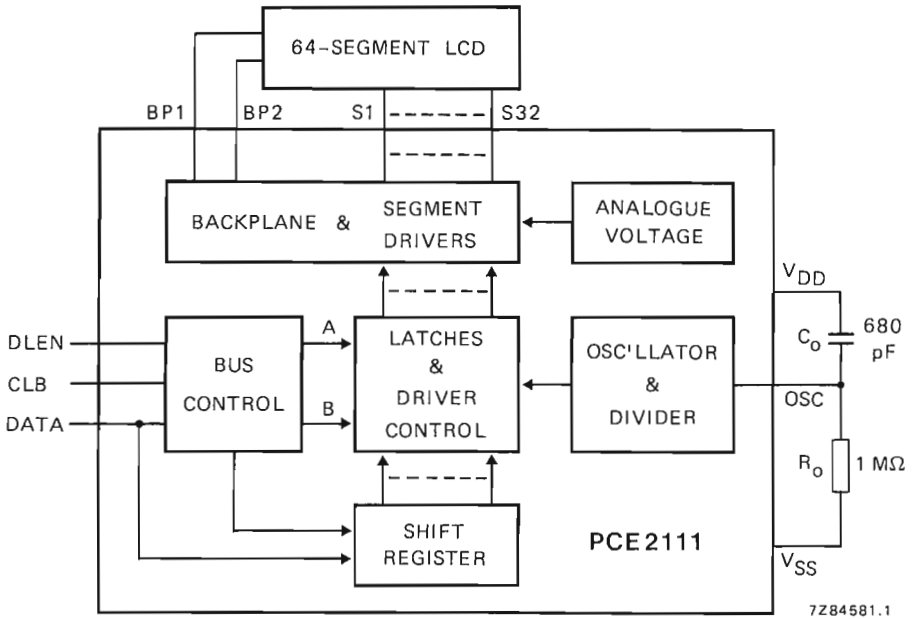


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCE2111P: 40-lead DIL; plastic (SOT-129).
PCE2111T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}	−0,3 to 8 V
Voltage on any pin	V_{SS}	−0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to + 85 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 85 °C; R_o = 1 MΩ; C_o = 680 pF; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	30	μA
Display frequency	see Fig. 8; T = 680 μs	f_{LCD}	60	80	100	Hz
D.C. component of LCD drive	with respect to V_{SX}	V_{BP}	–	± 10	–	mV
Load on each segment driver			–	–	10	MΩ
			–	–	500	pF
Load on each backplane driver			–	–	1	MΩ
			–	–	5	nF
Input voltage HIGH	see Fig. 9	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 9	V_{IL}	–	–	0,6	V
Rise time V_{BP} to V_{SX}	max. load	t_r	–	20	–	μs
Inputs CLB, DATA, DLEN	see note					
Input capacitance	for SOT-129 package	C_{IN}	–	–	10	pF
	for SOT-158A package	C_{IN}	–	–	5	pF
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	—	—	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	—	—	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	—	—	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	—	—	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	—	—	μs
Busy-time from load pulse to next start of transmission	see Fig. 3	t_{BUSY}	8	—	—	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	—	—	μs

Note

All times are measured with a voltage swing of minimum V_{IH} to V_{IL} (see Fig. 2). If external resistors are used in the bus lines (see Fig. 9), the extra time constant has to be added.

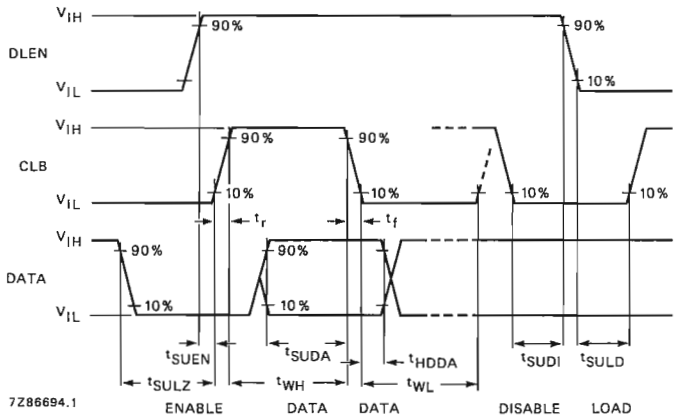


Fig. 2 CBUS timing.

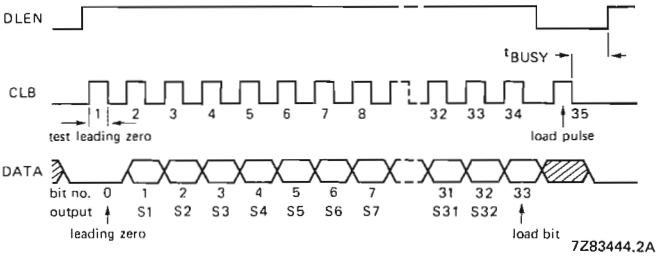


Fig. 3 CBUS data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If all test conditions are not fullfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

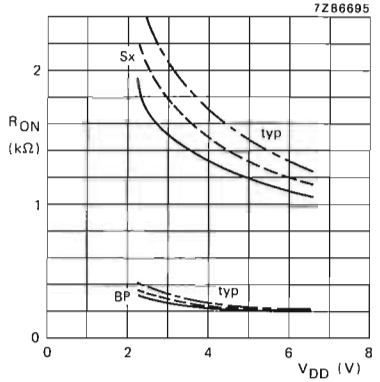


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = + 85 °C.

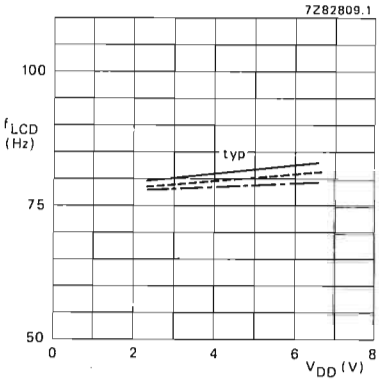


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 680 μs.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = + 85 °C.

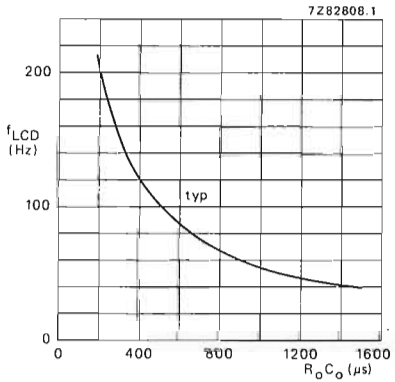


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

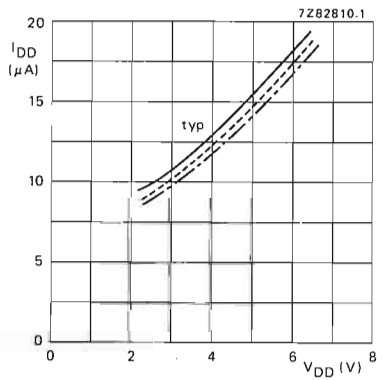


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = + 85 °C.

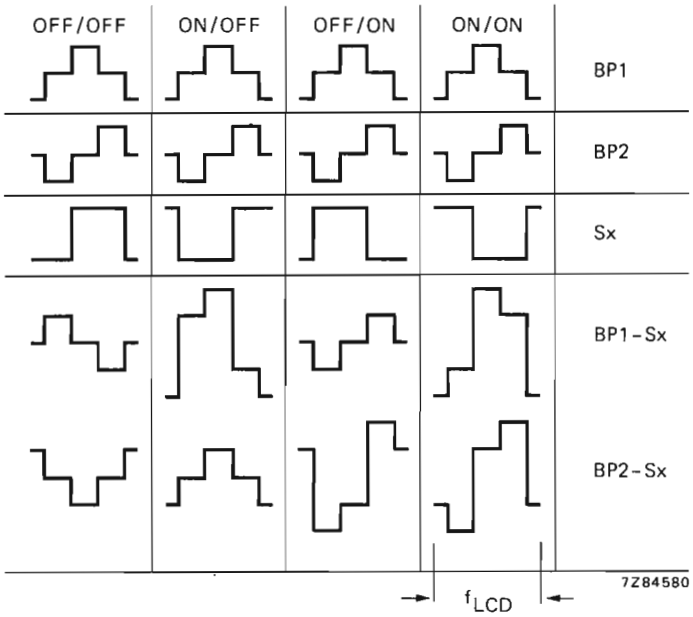


Fig. 8 Timing diagram.

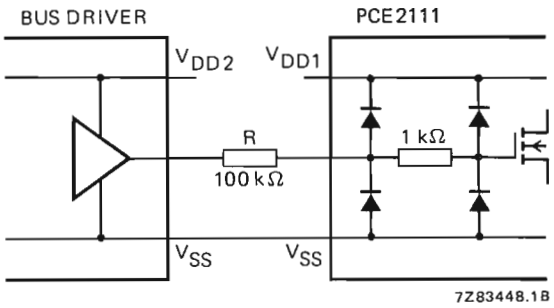


Fig. 9 Input circuitry.

Note to Fig. 9

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant$ 40 μA.

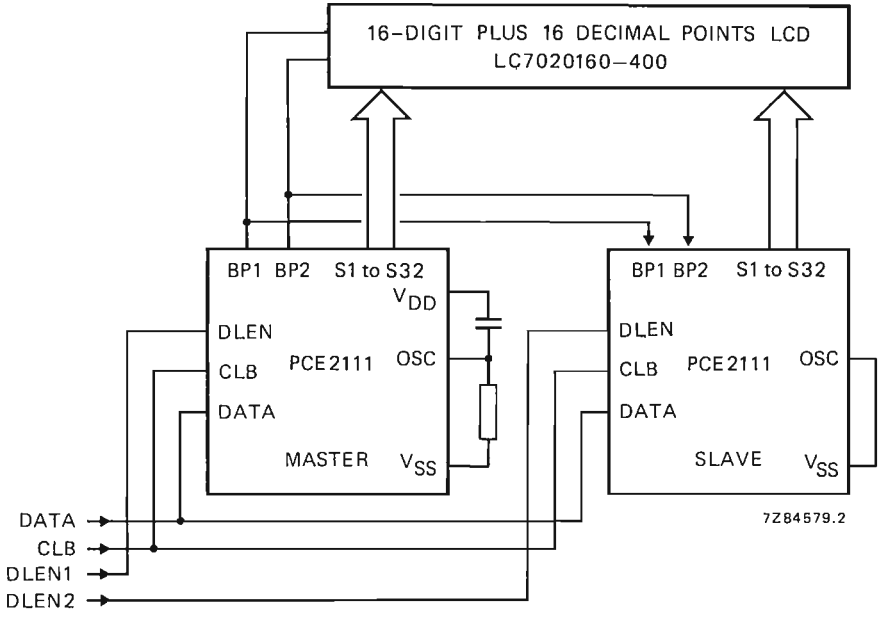


Fig. 10 Diagram showing expansion possibility for a 16-digit plus 16 decimal points LCD.

Note to Fig. 10

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCE2111, PCE2110 and PCE2100 ICs up to the BP drive capability of the master.

PCE2100 is a 40 LCD-segment driver; PCE2110 is a 60 LCD-segment driver plus 2 LED driver outputs.

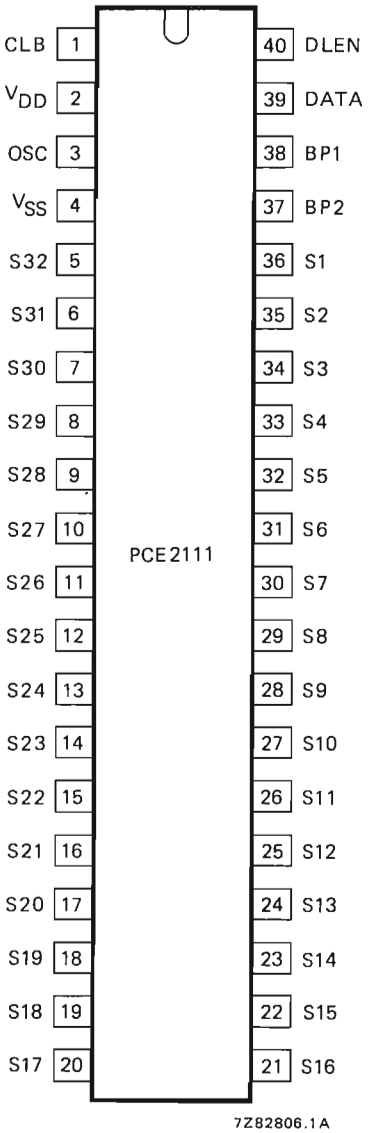


Fig. 11 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

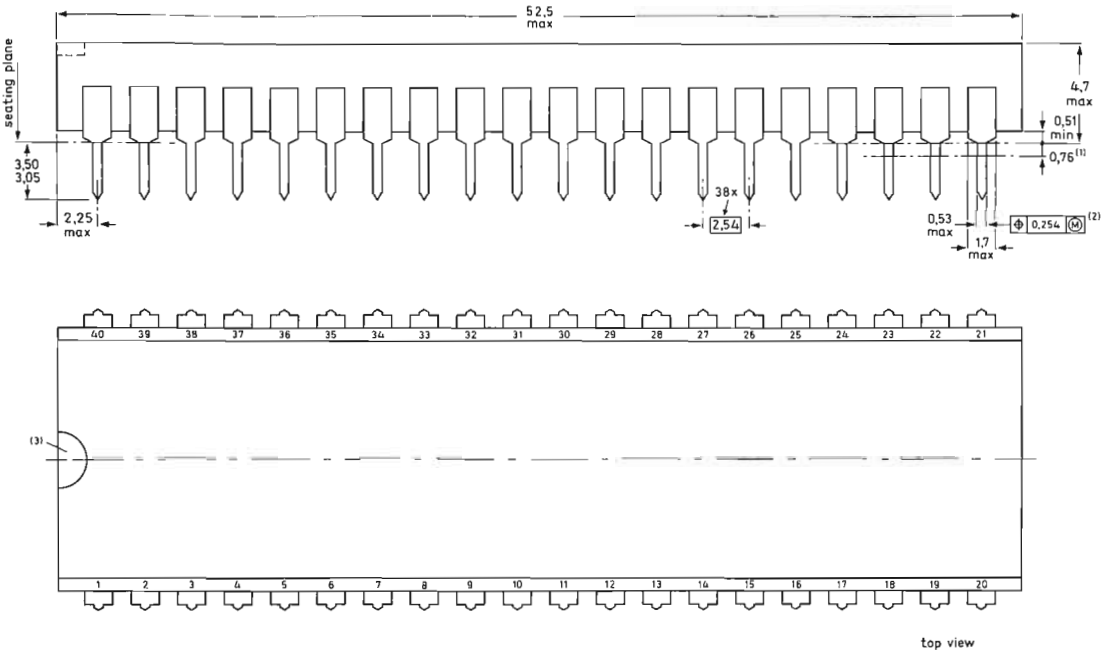
Outputs

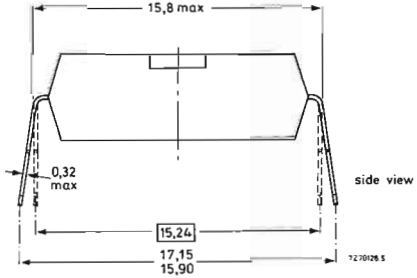
38	BP1	Backplane drivers (common of LCD)
37	BP2	Backplane drivers (common of LCD)
S1 to S32		LCD driver outputs

40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)

SOLDERING

See next page.





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

1. **By hand**

   Apply the soldering iron below the seating plane (or not more than 2 mm above it).
   If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

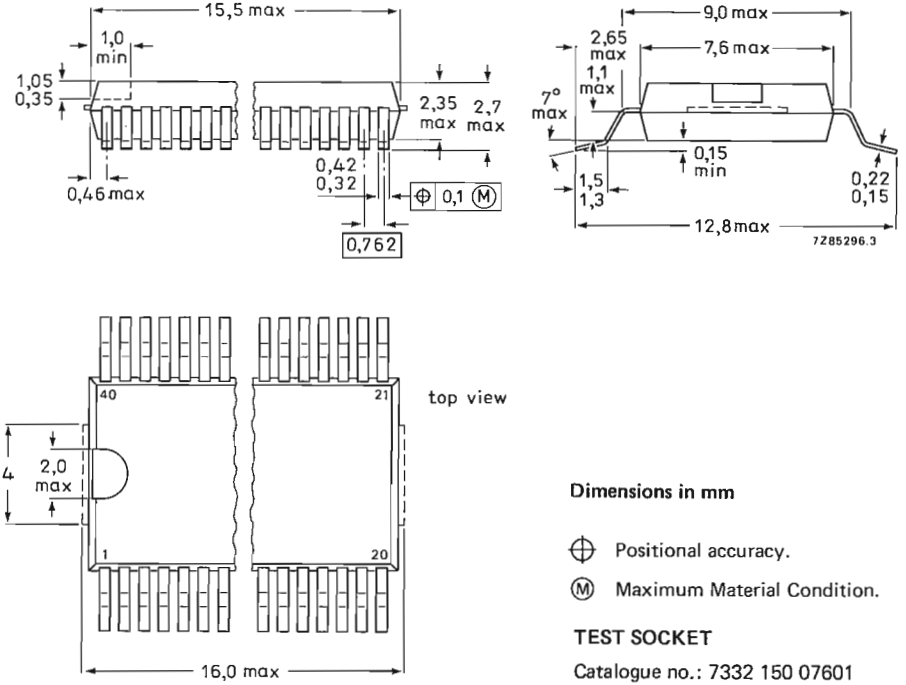
2. **By dip or wave**

   The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. **Repairing soldered joints**

   The same precautions and limits apply as in (1) above.

40-LEAD MINI-PACK; PLASTIC (VSO-40; SOT-158A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

TEST SOCKET

Catalogue no.: 7332 150 07601

SOLDERING

1. Soldering iron or pulse heated solder tool

Apply the heating tool to the flat part of the pin only.
Limit the contact time to maximum 10 seconds up to 300 °C, or 5 seconds up to maximum 400 °C.
When using the proper tools, up to 20 pins (at one side of the device) can be soldered in one operation with 2 to 5 seconds and 270 to 320 °C.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C. The permissible total time of immersing the whole package in the bath is 10 seconds, if it is allowed to cool down to less than 150 °C within 6 seconds.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.
If the vertical part of the pin needs heating, reduce the soldering iron temperature to 260 °C.

Note: the PCF8577 with I²C-bus interface will be available soon.

PROGRAMMABLE MULTI-TONE RINGER

The PCD3360 combined with a transducer (loudspeaker) and some external parts can replace the electro-mechanical bell in telephone sets. It meets European postal requirements, particularly with regard to over-voltage protection and input frequency selectivity. Moreover, since the loudspeaker is driven in class D, a transformer is not required.

Features

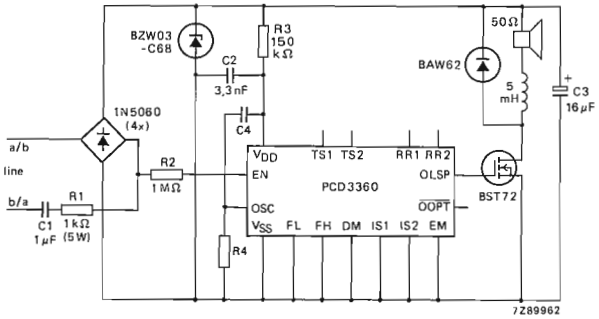
- 4 customer-defined mask-programmable tone sequences
- 4 selectable repetitive rates
- 3 selectable impedances
- 7 basic frequencies and a pause
- optional automatic swell in two steps
- programmable input-frequency limits
- mask-programmable waveform
- compatible with electro-dynamic and piezo-electric transducers
- output for optical signal

QUICK REFERENCE DATA

Non-repetitive peak-voltage	max. 5 kV
Continuous voltage on a-b input	max. 220 V
Available frequencies	533, 600, 667, 800, 1000, 1066 and 1333 Hz
Number of intervals per tone sequence	16 or 15
Lower frequency limits	13,33 or 20 Hz
Upper frequency limit	30 or 60 Hz
Impedance settings	7, 10,5 or 17,5 kΩ
Switch-on delay	max. 100 ms

Encapsulation: SOT-38 (16 pin DIL plastic)
SOT-97A (8-pin DIL plastic) optional

Application information



4-DIGIT/5-FUNCTION LCD WATCH CIRCUIT

GENERAL DESCRIPTION

The MJ123 is a single chip, silicon gate C-MOS watch circuit with five functions. It is designed to drive a 3½ or 4-digit, low voltage, liquid crystal display (LCD). Only two single-pole, single-throw switches are required to accomplish all display and setting functions. The circuit provides a full calendar function, which needs to be reset only once every four years. A bonding option allows the selection of 12-hour or 24-hour display mode.

Features

- Driving standard 3½ or a 4-digit LCD.
- 12 months calendar memory.
- One push button controls display.
- Using single 1,5 V battery.
- Displaying time, month-date or seconds.
- Additional alternating time-date display mode.
- Voltage doubler.
- Option for 12-hour/24-hour operation.
- Quartz crystal and trimmer are the only external oscillator components.

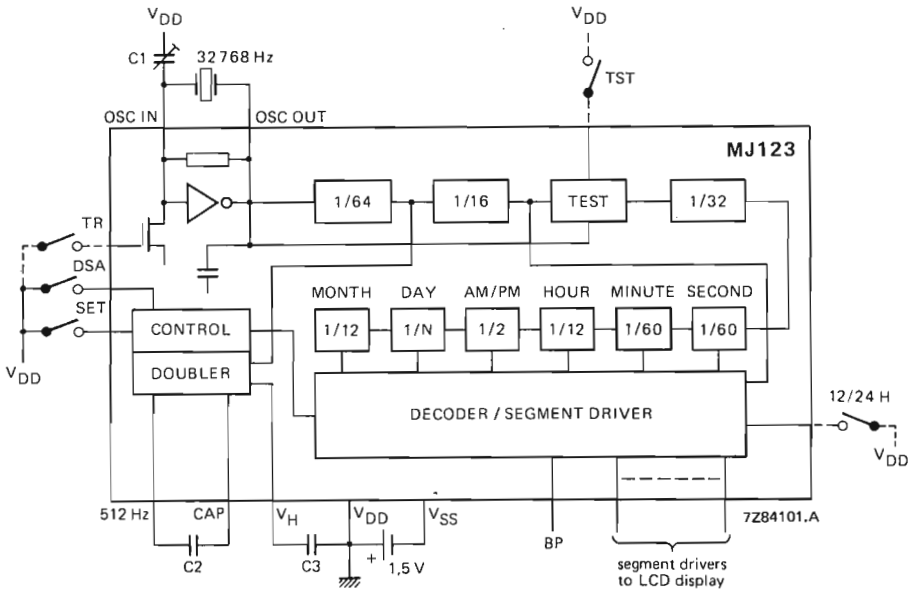
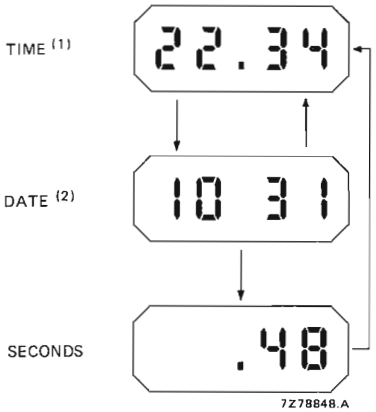


Fig. 1 Block diagram.

DISPLAY MODES



(1) 12-hour or 24-hour display operation.

Fig. 2 Examples of normal display modes.

All display and setting operations are controlled by two inputs, the display (DSA) input and the SET input. For normal operation only input DSA is used. Both inputs have an internal pull-down so that single-pole, single-throw contacts may be used.

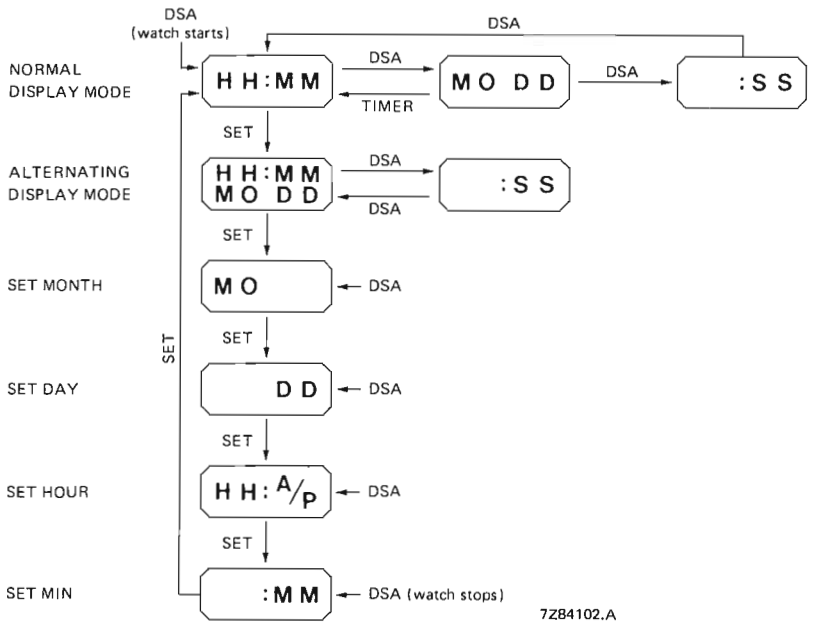


Fig. 3 Operation diagram.

Normal display mode

In this mode the HOURS-MINUTES will be displayed continuously with flashing colon. By pressing the DSA button, the circuit will display MONTH-DATE for two seconds and return to HOURS-MINUTES automatically. If display of MONTH-DATE in excess of 2 seconds is desired, the DSA button is held in the depressed condition for the required time period. For SECONDS display push the DSA button twice within 2 seconds. By pressing DSA a third time, the read-out will return to HOURS-MINUTES.

Alternating display mode

By pressing the SET button once, the watch will alternately display HOURS-MINUTES then MONTH-DATE for one second intervals. Depressing DSA will call-up seconds, depressing DSA again restores the alternating display mode.

Set mode

Detailed setting procedure:

To set the watch, use the following procedure (normal display mode is assumed):

1. Depress the SET button; circuit will advance to the alternating TIME/DATE display mode.
2. Depress the SET button until the display shows MONTH (shown in most-left digits). Release the SET button.
3. Depress the DSA button to advance MONTH to the proper value. Release the DSA button.
4. Depress the SET button until the display shows DATE (in most-right digits). Release the SET button.
5. Depress the DSA button to advance DATE to the proper value. Release the DSA button.
6. Depress the SET button until the display shows HOURS (shown in the most-left digits); A or P is shown in the most-right digit (12-hour mode only). Release the SET button.
7. Depress the DSA button to advance HOURS to the proper value. Release the DSA button.
8. Depress the SET button until the display shows MINUTES (shown in the most-right digits) and colon. Release the SET button.
9. Depress the DSA button to advance MINUTES to approximately one minute past the present time. Release the DSA button. Depressing the DSA button also resets the seconds-counter to zero and hold.
10. Depress SET button until the display shows HOURS and MINUTES. Release the SET button (the watch is still on hold).
11. When the time reaches the start of the minute (set in step 9 and shown on the display), depress the DSA button. The seconds-counter is then restarted and the watch is in the normal display mode.

12-hour/24-hour operation

A bonding option allows the selection of either 12-hour or 24-hour operation. If terminal '12/24H' is left open, the circuit operates in the 12-hour cycle, if this terminal is connected to V_{DD}, 24-hour operation is maintained.

Voltage doubler

The circuit has a built-in voltage doubler (for LCD driving), which needs two external capacitors C2 and C3 (see Fig. 1).

Testing

A test input (TST) is furnished to facilitate high-speed testing of the chip. A test reset input (TR) resets the circuit in a defined state: January 1st, 1:00 (AM)00 seconds for the 12-hour operation and 0:00(AM) for the 24-hour operation. Both inputs have an internal pull-down which allows these inputs to float during normal operation.
For segment test (all segments on), both DSA and SET have to be connected to V_{DD} at the same time, afterwards the watch is in the reset state.

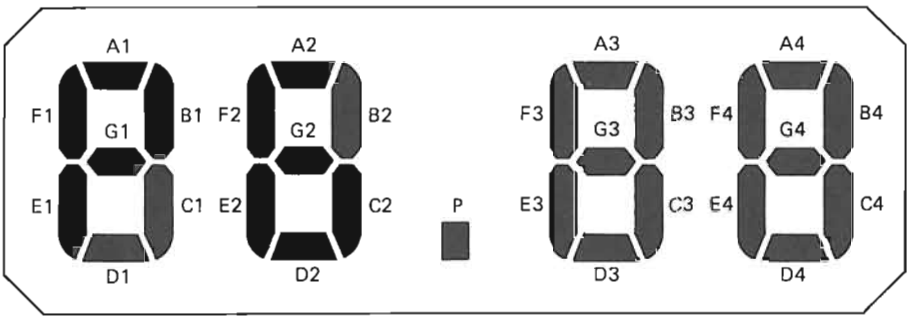


Fig. 4 Segment designation of LCD.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}	max.	2 V
Supply voltage with respect to V_H	V_{DD}	max.	4 V
Voltage on terminals OSCIN, OSCOUT, 512 Hz, SET, DSA, TST		max.	V_{DD} + 0,3 to V_{SS} −0,3 V
Voltage on terminal CAP		max.	V_{SS} + 0,3 to V_H −0,3 V
Voltage on all other terminals		max.	V_{DD} + 0,3 to V_H −0,3 V
Storage temperature	T_{stg}		−55 to + 125 °C
Operating ambient temperature	T_{amb}		−10 to + 70 °C

CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −1,5 V; T_{amb} = 25 °C; quartz crystal parameters: f = 32 768 Hz, $R_{s\,max}$ = 40 kΩ; C_L = 8 to 10 pF.

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage		V_{SS}	−1,2	–	−1,7	V
Segment driver output resistance (both states)	I_O = 10 μA		–	20	–	kΩ
Back-plane driver output resistance (both states)	I_O = 10 μA		–	1	–	kΩ
512 Hz output resistance (both states)	I_O = 10 μA		–	6	–	kΩ
Supply current	C2 = C3 = 50 nF no loads connected	I_{SS}	–	1,2	2,5	μA
Display driver voltage	C2 = C3 = 50 nF	V_H	–	2,8	–	V
Input current DSA; SET	input connected to V_{DD}; V_H = −3 V		10	30	60	μA
Input current 12/24 H	input connected to V_{DD}; V_H = −3 V		–	0,1	–	μA
Oscillator polarization resistance			5	15	50	MΩ
Oscillator output capacitance			–	40	–	pF

DEVELOPMENT SAMPLE DATA

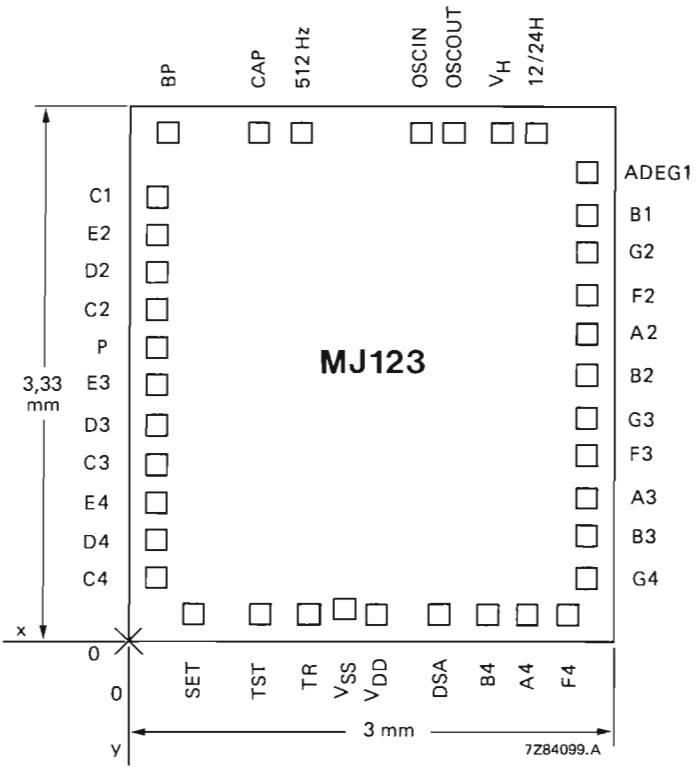


Fig. 5 Bonding pad locations; 38 terminals.

SET	setting sequence advance button
DSA	date, seconds, display/counter advance button
TR	test reset
V_{SS}	supply voltage (−1,5 V)
V_H	supply voltage LCD driver (−3,0 V)
V_{DD}	most positive supply voltage (0 V)
TST	high-speed test control input
BP	32 Hz back-plane driver (common of LCD display)
CAP, 512 Hz	voltage doubler capacitor terminals
OSCIN	input of oscillator inverter
OSCOUT	output of oscillator inverter
12/24H	selects 12-hour or 24-hour operation

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0).

Dimensions in μm

pad	x	y		pad	x	y	
SET	400	150	bottom	G4	2830	400	right
TST	810	|	|	B3	|	660	|
TR	1120	150	|	A3	|	910	|
V_{SS}	1320	180	|	F3	|	1160	|
V_{DD}	1530	150	|	G3	|	1410	|
DSA	1920	|	|	B2	|	1660	|
B4	2210	|	|	A2	|	1920	|
A4	2470	|	|	F2	|	2170	|
F4	2720	150	bottom	G2	|	2420	|
				B1	|	2670	|
				ADEG1	2830	2920	right
BP	240	3180	top	C4	150	400	left
CAP	790	|	|	D4	|	630	|
512 Hz	1070	|	|	E4	|	870	|
OSCIN	1800	|	|	C3	|	1110	|
OSCOUT	2010	|	|	D3	|	1350	|
V_H	2310	|	|	E3	|	1590	|
12/24H	2520	3180	top	P	|	1830	|
				C2	|	2065	|
				D2	|	2300	|
				E2	|	2540	|
				C1	150	2780	left

DEVELOPMENT SAMPLE DATA

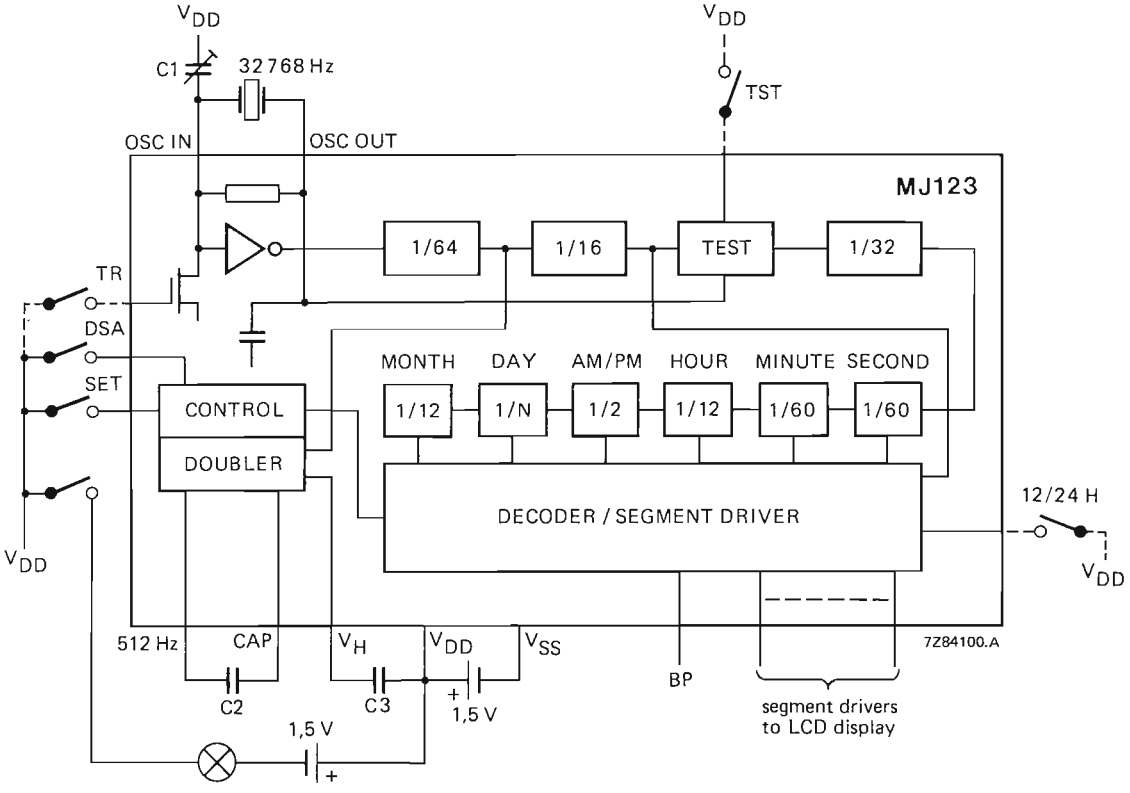


Fig. 6 Circuit diagram showing operation with two 1,5 V batteries, voltage doubler and 1,5 V lamp. C1 = 5 to 30 pF; C2 = 20 to 50 nF.

N.B.: Circuit diagram with single 1,5 V battery and voltage doubler see Fig. 1; C1 and C2 as Fig. 6.

OTHER COMPONENTS FOR TELEPHONE SUBSCRIBER SETS

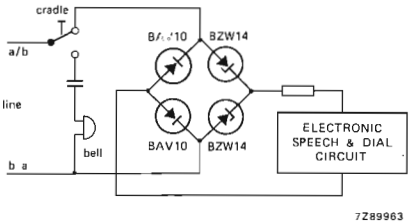
TRANSIENT SUPPRESSOR DIODE

The BZW14 is a zener diode suitable for transient suppression in telephony equipment.

QUICK REFERENCE DATA

Maximum stand-off voltage	12 V
Maximum clamping voltage at 50 A peak (6/320 μs)	28 V
Maximum non-repetitive peak reverse current	50 A
Maximum leakage current at maximum stand-off voltage	40 μA
Encapsulation	SOD-64

APPLICATION DIAGRAM



For lower forward voltage-drop across the bridge, two Schottky-barrier diodes BAT85 may be used instead of the BAV10 diodes.

PTC THERMISTOR

For use as a current stabilizer to compensate for variations in telephone line resistance.

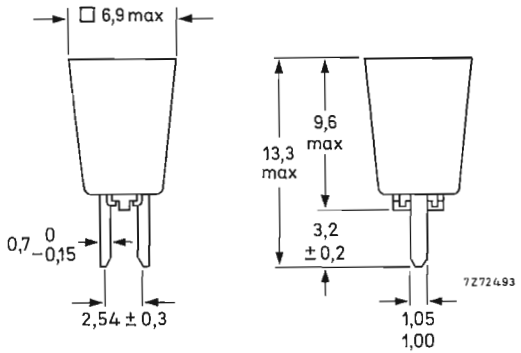
QUICK REFERENCE DATA

Resistance at 25 °C	115 Ω ± 25 Ω
Minimum resistance at 155 °C (V_{pulse} = 33 V)	15 kΩ
Typical switching temperature	97 °C
Minimum temperature coefficient	10%/°C
Maximum d.c. voltage	33 V
Operating temperature range	
at zero power	−25 °C to + 155 °C
at maximum voltage	+ 5 °C to + 55 °C

MECHANICAL DATA

Dimensions in mm

Outlines



PTC THERMISTOR

For use as a current stabilizer to compensate for variations in telephone line resistance.

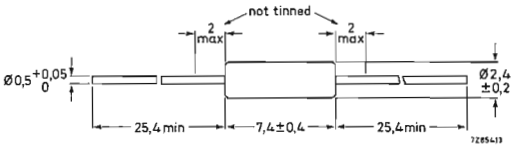
QUICK REFERENCE DATA

Resistance at 25 °C	120 Ω ± 30 Ω
Typical switching temperature	150 °C
Minimum temperature coefficient	8%/°C
Maximum d.c. voltage	34 V
Maximum response	2 s
Operating temperature range	
at zero power	−25 °C to + 155 °C
at maximum voltage	+ 5 to + 55 °C

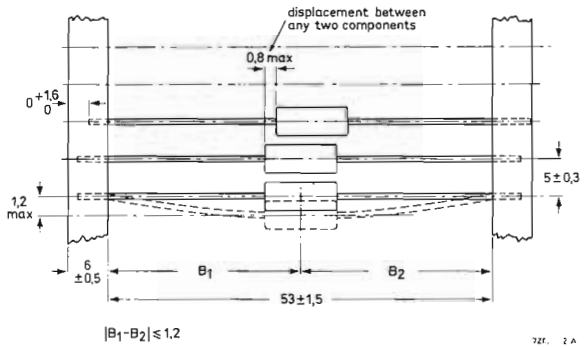
MECHANICAL DATA

Dimensions in mm

Outlines: SOD-27



Configuration of bandolier



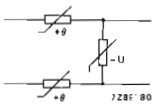
PVP MODULES

For protection of telephony equipment against lightning and direct contact with external voltages. They each comprise two PTC thermistors electrically and thermally coupled to a voltage-dependent resistor.

QUICK REFERENCE DATA

	...91001	...91002
Maximum non-repetitive transient current I_{max}	25 A (8/20 μs)	25 A (8/20 μs)
Maximum voltage at I_{max}	250 V	310 V
Typical R_{PTC} @ T_{amb} = 70 °C	2 x 20 Ω	2 x 20 Ω
Maximum continous I_{PTC} @ T_{amb} = 70 °C	60 mA	60 mA
Maximum response at $I_{PTC} > 1,5$ A	3 s	3 s
Input current (supply 220 V via 20 Ω)	15 mA	15 mA

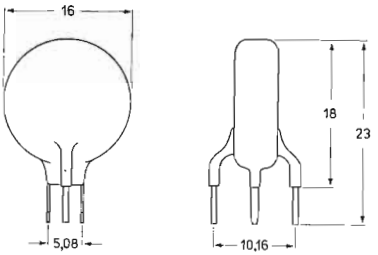
CIRCUIT DIAGRAM

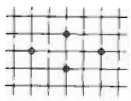


MECHANICAL DATA

Dimensions in mm

Outlines





VOLTAGE DEPENDENT RESISTOR

metal oxide disc

For protection of telephone sets with current loop interrupt dialling.

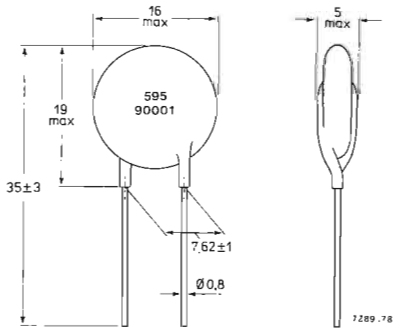
QUICK REFERENCE DATA

Maximum non-repetitive transient current I_{max} (1/700 μs)	25 A
Maximum voltage at I_{max}	285 V
Minimum low-current voltage	60 V @ 10 μA 130 V @ 1 mA

MECHANICAL DATA

Dimensions in mm

Outlines



VOLTAGE DEPENDENT RESISTOR

metal oxide disc

For protection of telephone sets with current-loop interrupt dialling.

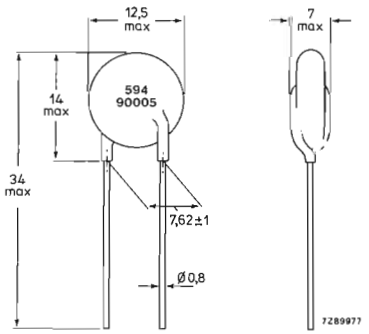
QUICK REFERENCE DATA

	90005	90008	90009
Maximum non-repetitive transient current I_{max}	22 A (7/700 μs)	55 A (8/20 μs)	50 A (8/20 μs)
Maximum voltage at I_{max}	200 V	160 V	230 V
Minimum low-current voltage	103 V @ 0,1 mA	68 V @ 10 μA	100 V @ 1 mA

MECHANICAL DATA

Dimensions in mm

Outlines



VOLTAGE DEPENDENT RESISTOR

metal oxide disc

For protection of telephone sets with current loop interrupt dialling.

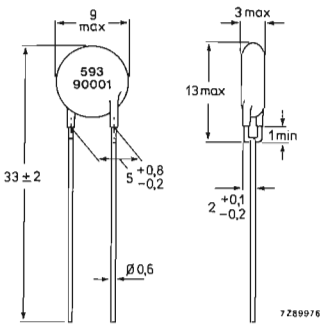
QUICK REFERENCE DATA

Maximum non-repetitive transient current I_{max} (8/20 μs)	22 A
Maximum voltage at I_{max}	200 V
Minimum low-current voltage	90 V @ 1 mA

MECHANICAL DATA

Dimensions in mm

Outlines



N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

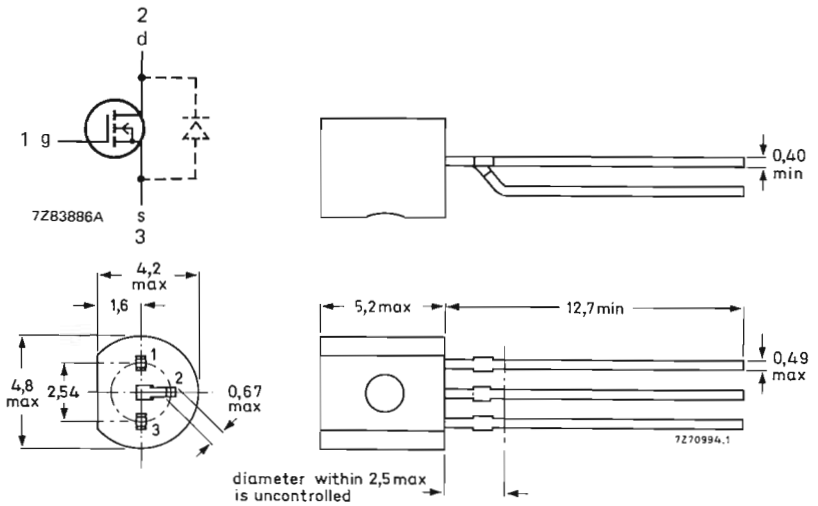
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,3 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0,83 W
Drain-source ON-resistance I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. <	7 Ω 10 Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	150 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	600 mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	0,83 W
Storage temperature	T_{stg}	−65 to	+150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$		150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	<	1,0 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100 nA
Gate-source cut-off voltage I_D = 1,0 mA; V_{DS} = V_{GS}	$V_{(P)GS}$	> <	1,5 V 3,5 V
Drain-source ON-resistance (see Fig. 4) I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. <	7 Ω 10 Ω
Transfer admittance at f = 1 kHz I_D = 200 mA; V_{DS} = 5 V	$\lvert y_{fs} \rvert$	typ.	150 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ.	15 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ.	13 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	3 pF
Switching times (see Figs 2 and 3) I_D = 200 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. <	4 ns 10 ns
	t_{off}	typ. <	4 ns 10 ns

* Transistor mounted on printed circuit board, max. lead length 4 mm.

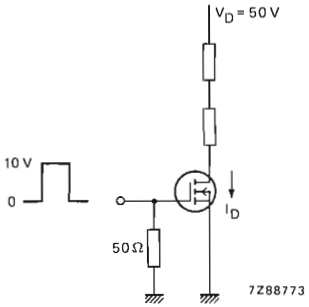


Fig. 2 Switching times test circuit.

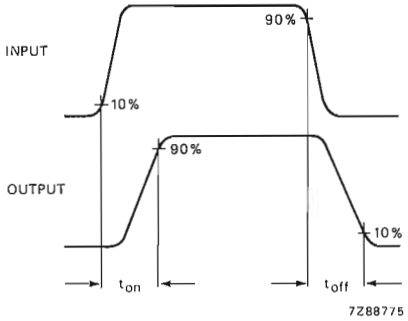


Fig. 3 Input and output waveforms.

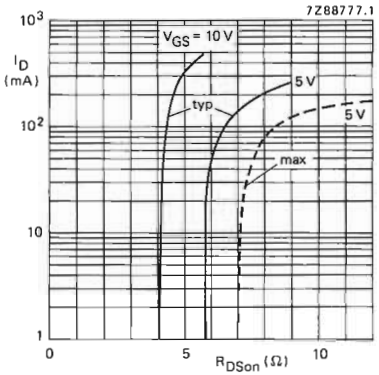


Fig. 4 T_j = 25 °C; typ. values.

Application information: see PCD3360

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use as line current interruptor in telephone sets and for application with relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

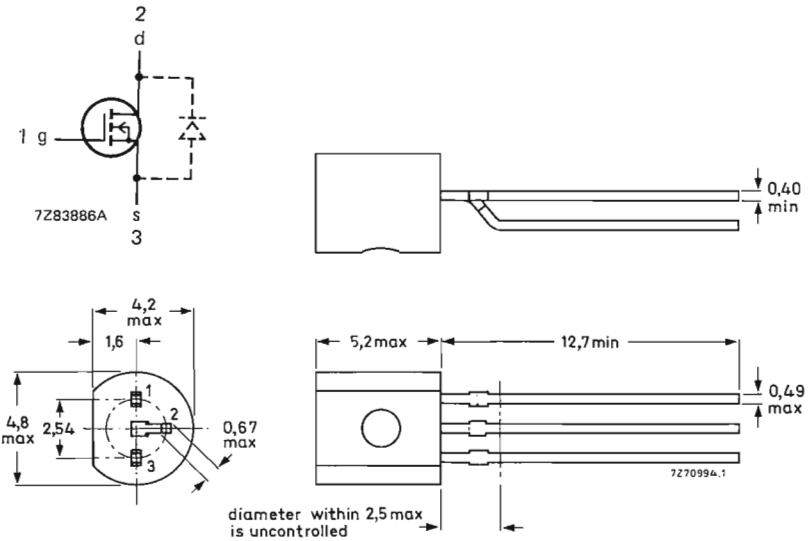
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,4 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	250 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	400 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	1 W
Storage temperature	T_{stg}	−65 to	+150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$		125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	<	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100 nA
Gate-source cut-off voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{(P)GS}$	> <	1,5 V 3,5 V
Drain-source ON-resistance (see Fig. 4) I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. min.	6 Ω 12 Ω
Transfer admittance at f = 1 kHz I_D = 400 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ.	30 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ.	25 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	6 pF
Switching times (see Figs 2 and 3) I_D = 400 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	<	10 ns
	t_{off}	<	15 ns

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

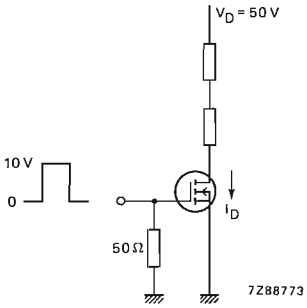


Fig. 2 Switching times test circuit.

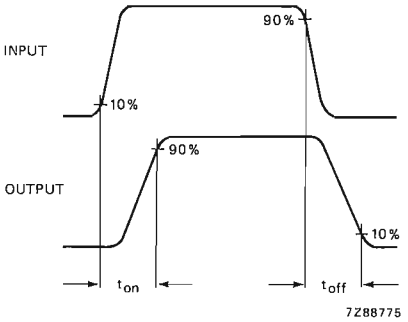


Fig. 3 Input and output waveforms.

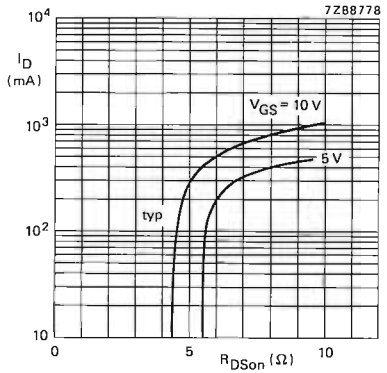


Fig. 4 T_j = 25 °C.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in TO-92 envelope and designed for use as line current interruptor in telephone sets and for application with relay, high-speed and line-transistor drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

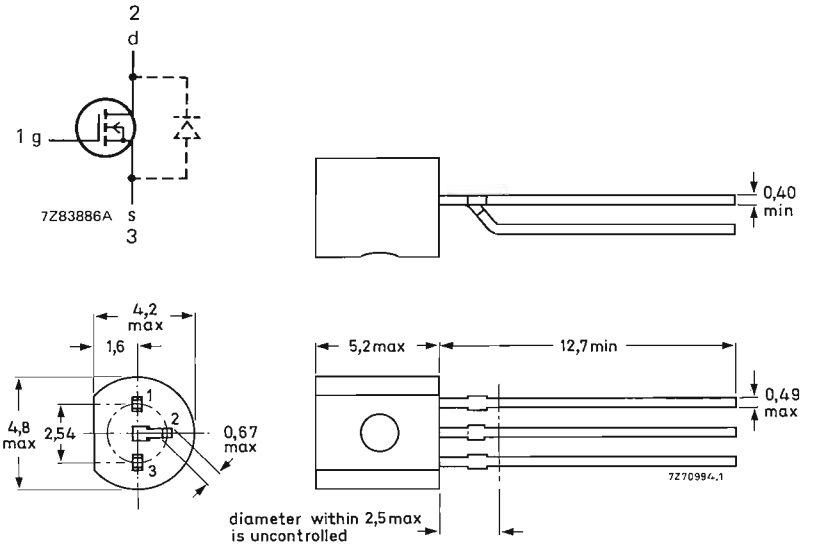
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	150 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,4 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1,0 W
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. <	7 Ω 10 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 15 V; f = 1 kHz	$\|y_{fs}\|$	typ.	250 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	150 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,4 A
Drain current (peak)	I_{DM}	max.	0,8 A
Total power dissipation*			
up to T_{amb} = 25 °C	P_{tot}	max.	1 W
up to T_{mb} = 50 °C	P_{tot}	max.	8 W
Storage temperature	T_{stg}	−65 to	+150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$		125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	150 V
Drain-source leakage current			
V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	<	10 μA
Gate-source leakage current			
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100 nA
Gate-source cut-off voltage			
I_D = 10 μA; V_{DS} = V_{GS}	$V_{(P)GS}$	>	0,5 V
		<	2,7 V
Drain-source ON-resistance (see Fig. 4)			
I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ.	7 Ω
		<	10 Ω
I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ.	6 Ω
Transfer admittance at f = 1 kHz			
I_D = 400 mA; V_{DS} = 5 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ.	30 pF
Output capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ.	25 pF
Feedback capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	6 pF
Switching times (see Figs 2 and 3)			
I_D = 400 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	<	10 ns
	t_{off}	<	15 ns

* Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

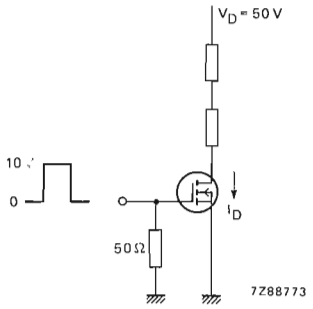


Fig. 2 Switching times test circuit.

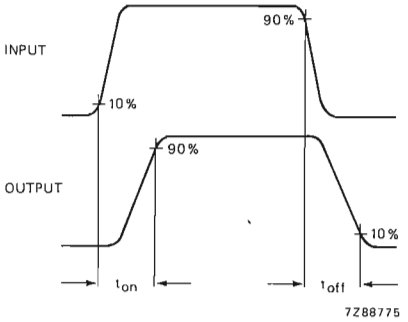


Fig. 3 Input and output waveforms.

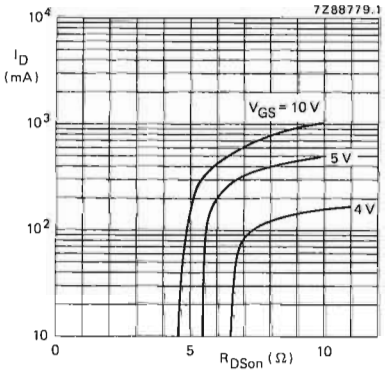


Fig. 4 T_j = 25 °C; typ. values.

1⅓ inch LOW POWER LOUDSPEAKER

APPLICATION

Extremely thin loudspeaker for personal agenda intercoms, telephones, and many other professional purposes.

TECHNICAL DATA

	version 8	15	25	
Rated impedance	8	15	25	Ω
Voice coil resistance	6,9	13,5	20,5	Ω
Rated frequency range		400 to 10 000		Hz
Resonance frequency		600		Hz
Power handling capacity, measured without filter, loudspeaker unmounted		0,3		W
Operating power (sound level 74 dB, 1 m)		55		mW
Sweep voltage (40 to 15 000 Hz)	1,1	1,5	1,9	V
Characteristic sensitivity		53		dB
Energy in air gap		3,4		mJ
Flux density		0,55		T
Air-gap height		0,8		mm
Voice coil height	2,7	2,7	2,9	mm
Core diameter		14,5		mm
Magnet material		rare earth		
mass		1,5		g
Mass of loudspeaker		7		g

Connection is by soldering (max. 350 °C for 3,5 s). The loudspeaker has a plastic frame and a polycarbonate membrane.

Dimensions in mm

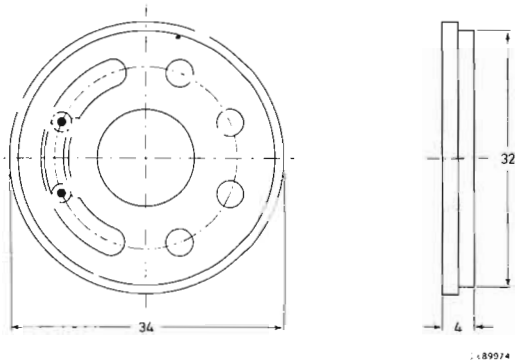


Fig. 1.

One tag has a red mark to facilitate phase matching. Recommended baffle hole: ϕ 29 mm.

AVAILABLE VERSIONS

AD01980/Z8 catalogue number 2403 256 12323
AD01980/Z15 catalogue number 2403 256 12322
AD01980/Z25 catalogue number 2403 256 12321

These numbers are for bulk-packed loudspeakers.

FREQUENCY RESPONSE CURVES (see Fig. 2)

Curve of sound pressure, measured in anechoic room at the operating power.

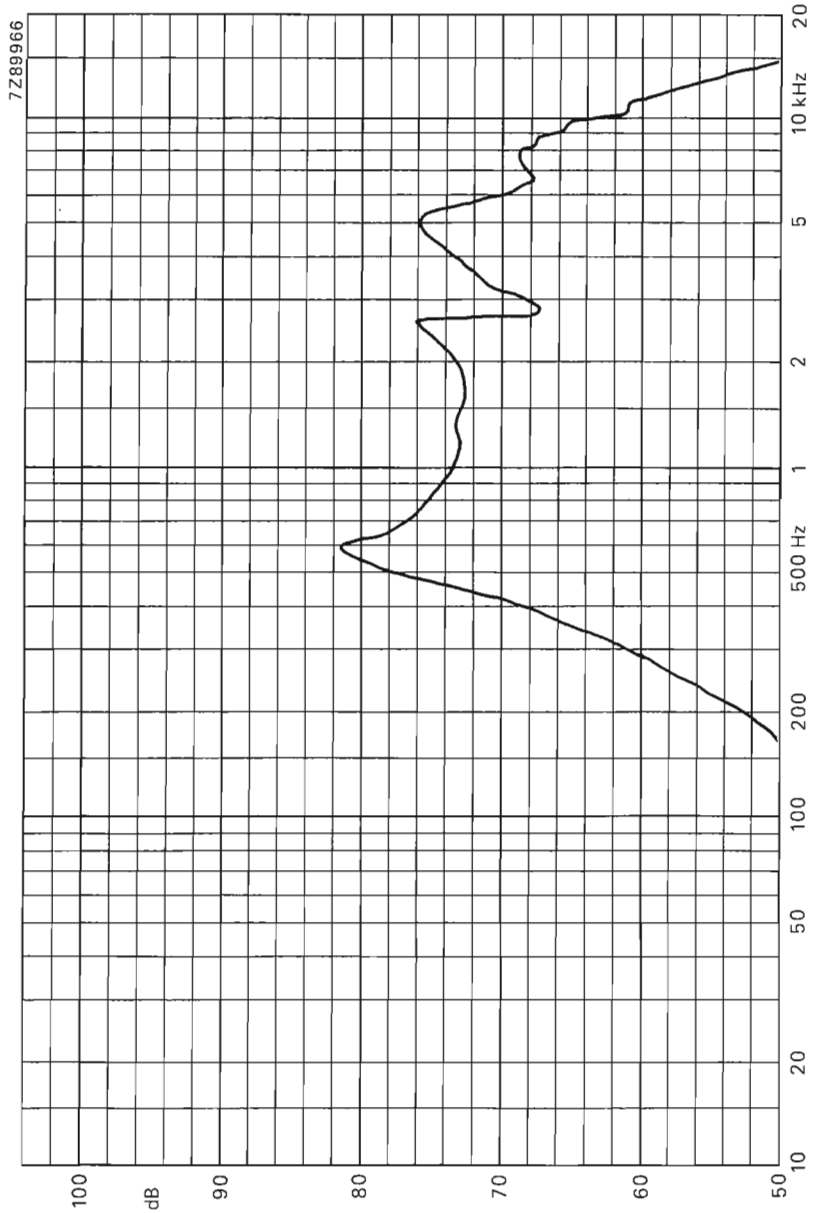


Fig. 2.

1½ inch LOW POWER LOUDSPEAKER

APPLICATION

Extremely thin loudspeaker for personal agenda intercoms, telephones, and many other professional purposes.

TECHNICAL DATA

	version 8	15	25	
Rated impedance	8	15	25	Ω
Voice coil resistance	6,9	13,5	20,5	Ω
Rated frequency range		400 to 10 000		Hz
Resonance frequency		600		Hz
Power handling capacity, measured without filter, loudspeaker unmounted		0,3		W
Operating power (sound level 74 dB, 1 m)		50		mW
Sweep voltage (40 to 15 000 Hz)	1,1	1,5	1,9	V
Characteristic sensitivity		54		dB
Energy in air gap		3,4		mJ
Flux density		0,55		T
Air-gap height		0,8		mm
Voice coil height	2,7	2,7	2,9	mm
Core diameter		14,4		mm
Magnet material		rare earth		
mass		1,5		g
Mass of loudspeaker		7,5		g

Connection is by soldering (max. 350 °C, for 3,5 s). The loudspeaker has a plastic frame and a polycarbonate membrane.

Dimensions in mm

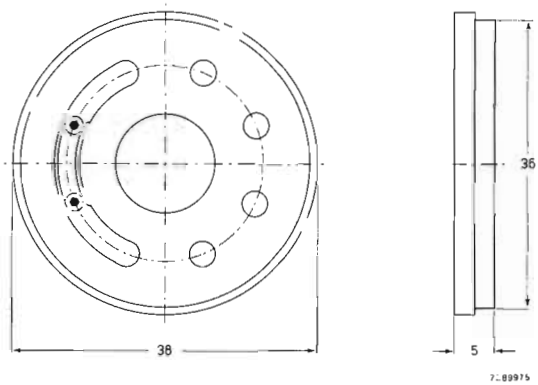


Fig. 1.

One tag has a red mark to facilitate phase matching. Recommended baffle hole: ϕ 33 mm.

AVAILABLE VERSIONS

AD01985/Z8 catalogue number 2403 256 12223
AD01985/Z15 catalogue number 2403 256 12222
AD01985/Z25 catalogue number 2403 256 12221

These numbers are for bulk-packed loudspeakers.

FREQUENCY RESPONSE CURVES (see Fig. 2)

Curve of sound pressure, measured in anechoic room at the operating power.

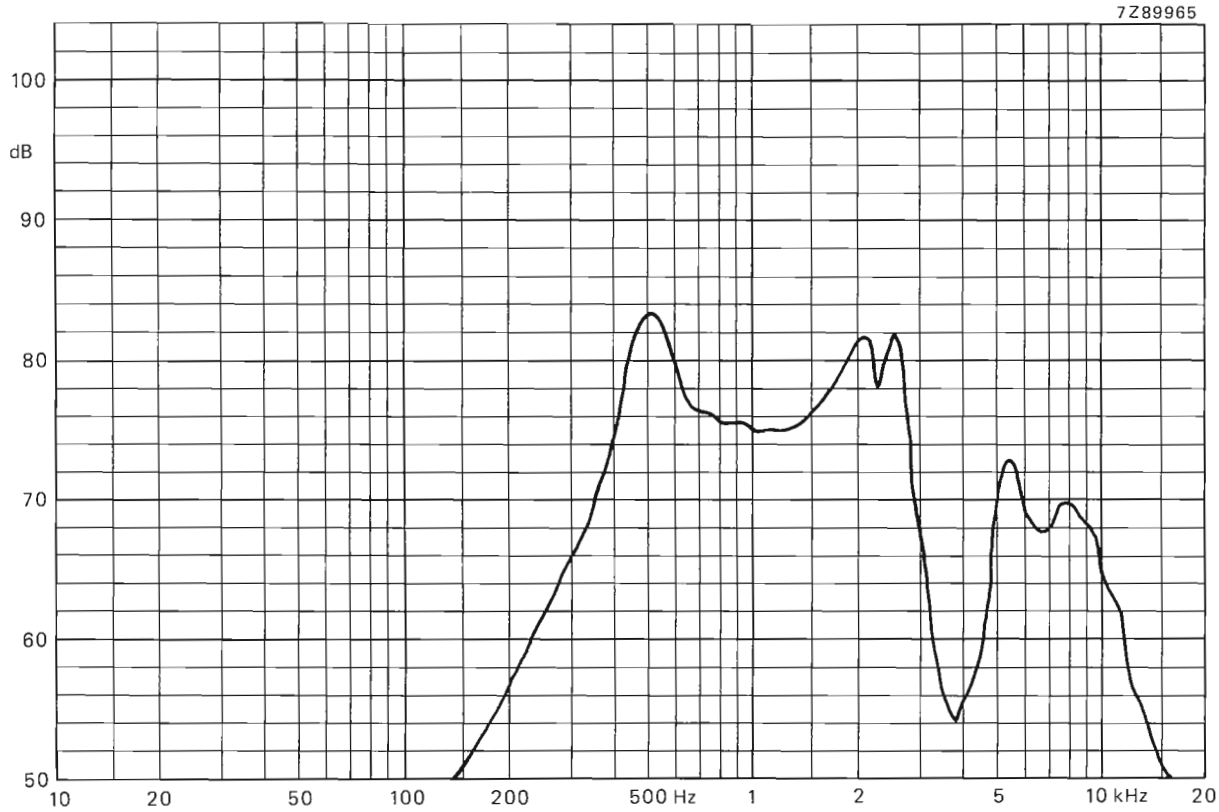


Fig. 2.

2½ INCH LOW POWER LOUDSPEAKER

APPLICATION

For portable receivers and intercoms.

TECHNICAL DATA

	version						
	Z4	Z8	Z15	Z25	Z50	Z150	
Rated impedance	4	8	15	25	50	150	Ω
Voice coil resistance	3,5	7,1	13,7	22,8	37	127	Ω
Rated frequency range			180 to 4000				Hz
Resonance frequency			360				Hz
Power handling capacity, loudspeaker unmounted, measured without filter			1				W
Operating power (sound level 90 dB, 0,5 m)			0,55				W
Sweep voltage (frequency range: 240 to 15000 Hz)	1	1,4	1,9	2,5	5	8,7	V
Energy in air gap			12,7				mJ
Flux density			0,74				T
Air-gap height			2,5				mm
Voice coil height	2,7	2,2	3,0	3,6	3,9	3,5	mm
Core diameter			10				
Magnet material			ceramic				
diameter			28,5				mm
mass			0,018				kg
Mass of loudspeaker			0,05				kg

The loudspeaker has a plastic frame, and a paper cone and surround. Connection to the loudspeaker by means of 2,8 mm (0,11 inch) tag connectors or by soldering.

Dimensions (mm)

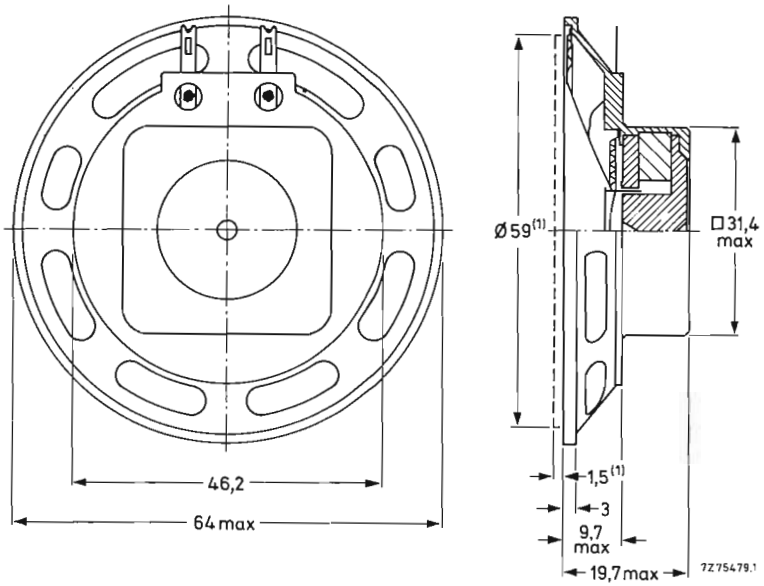


Fig.1.

(1) Baffle hole and clearance depth required for cone movement at the specified power handling capacity.

One tag is indicated by + sign for in-phase connection.

AVAILABLE VERSIONS

AD2071/Z4, catalogue number 2403 257 23821
AD2071/Z8, catalogue number 2403 257 23822
AD2071/Z15, catalogue number 2403 257 23823
AD2071/Z25, catalogue number 2403 257 23824
AD2071/Z50, catalogue number 2403 257 23826
AD2071/Z150, catalogue number 2403 257 23825

these numbers apply to bulk packed loudspeakers, minimum packing quantity 125 per unit.

FREQUENCY RESPONSE CURVE (see Fig. 2)

Sound pressure measured in anechoic room, loudspeaker mounted on IEC baffle.

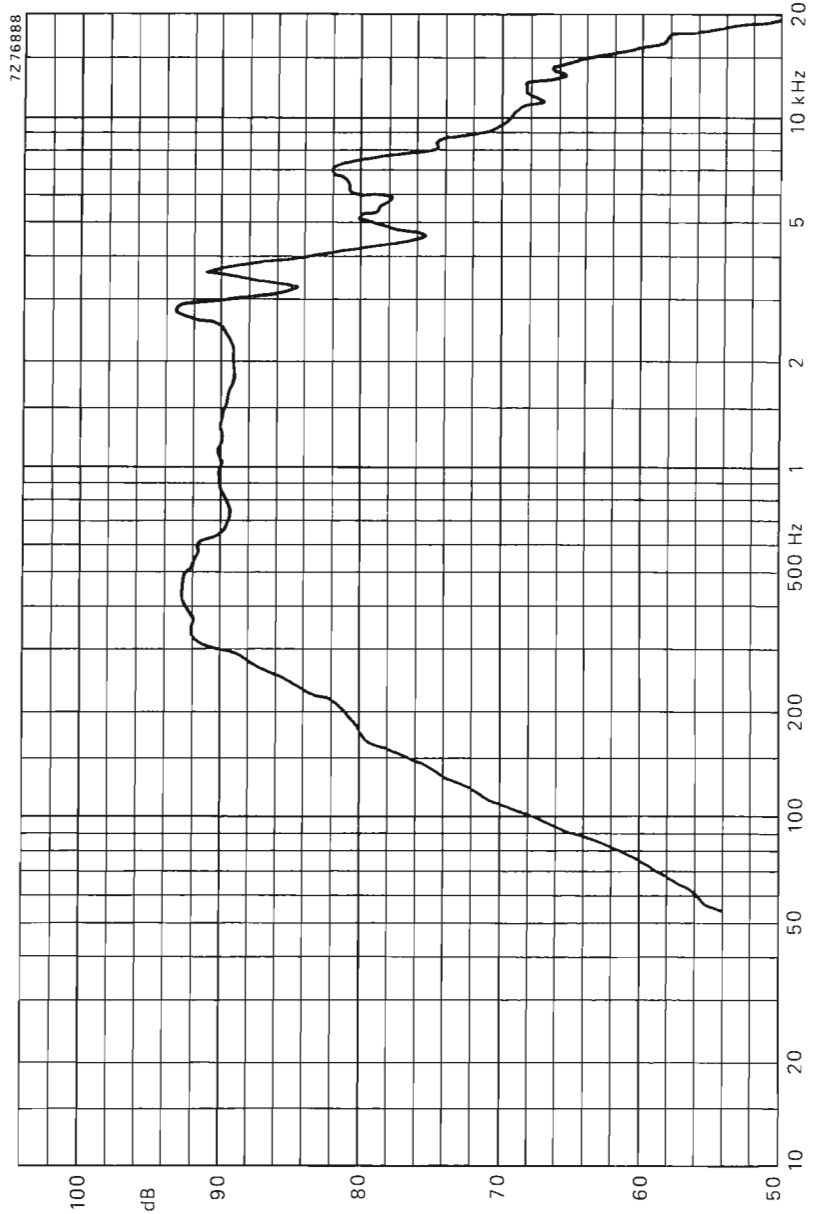


Fig.2.

3 INCH LOW POWER LOUDSPEAKERS

APPLICATION

For portable receivers and intercoms.

TECHNICAL DATA

	version						
	Y4	Y8	Y15	Y25	Y50	Y150	
Rated impedance	4	8	15	25	50	150	Ω
Voice coil resistance	3,5	7,1	13,7	22,8	45	127	Ω
Rated frequency range	100 to 6000						Hz
Resonance frequency	250						Hz
Power handling capacity, loudspeaker unmounted, measured without filter	2						W
Operating power (sound level 90 dB, 0,5 m)	0,6						W
Sweep voltage (frequency range 170 to 15 000 Hz)	2	2,8	3,9	5	7,1	12,2	V
Energy in air gap	12,7						mJ
Flux density	0,74						T
Air-gap height	2,5						mm
Voice coil height	2,7	2,2	3,0	3,6	4,7	3,5	mm
Core diameter	10						mm
Magnet material	ceramic						
diameter	28,5						mm
mass	0,018						kg
Mass of loudspeaker	0,059						kg

The loudspeakers have a plastic frame, and a paper cone and surround. Type AD3371/Y. is provided with 4 mounting ears (dotted in Fig. 1). Connection to the loudspeakers by means of 2,8 mm (0,11 inch) tag connectors or by soldering.

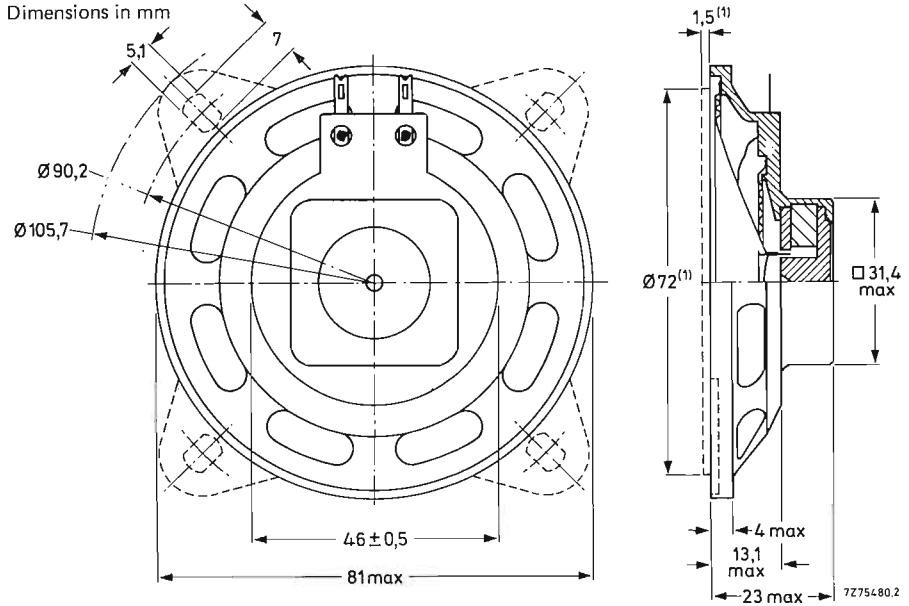


Fig. 1 Dotted mounting ears for type AD3371/Y.

(1) Baffle hole and clearance depth required for cone movement at the specified power handling capacity.

One tag is indicated by a red mark for in-phase connection.

AVAILABLE VERSIONS

AD3071/Y4,	catalogue number 2403 257 23621
AD3071/Y8,	catalogue number 2403 257 23622
AD3071/Y15,	catalogue number 2403 257 23623
AD3071/Y25,	catalogue number 2403 257 23624
AD3071/Y50,	catalogue number 2403 257 23625
AD3071/Y150,	catalogue number 2403 257 23626
AD3371/Y4,	catalogue number 2403 257 23521
AD3371/Y8,	catalogue number 2403 257 23522
AD3371/Y15,	catalogue number 2403 257 23523
AD3371/Y25,	catalogue number 2403 257 23524
AD3371/Y50,	catalouge number 2403 257 23525
AD3371/Y150,	catalogue number 2403 257 23526

these numbers apply to bulk packed loudspeakers, minimum packing quantity 50 per unit.

FREQUENCY RESPONSE CURVE (see Fig. 2)

Sound pressure measured in anechoic room, loudspeaker mounted on IEC baffle.

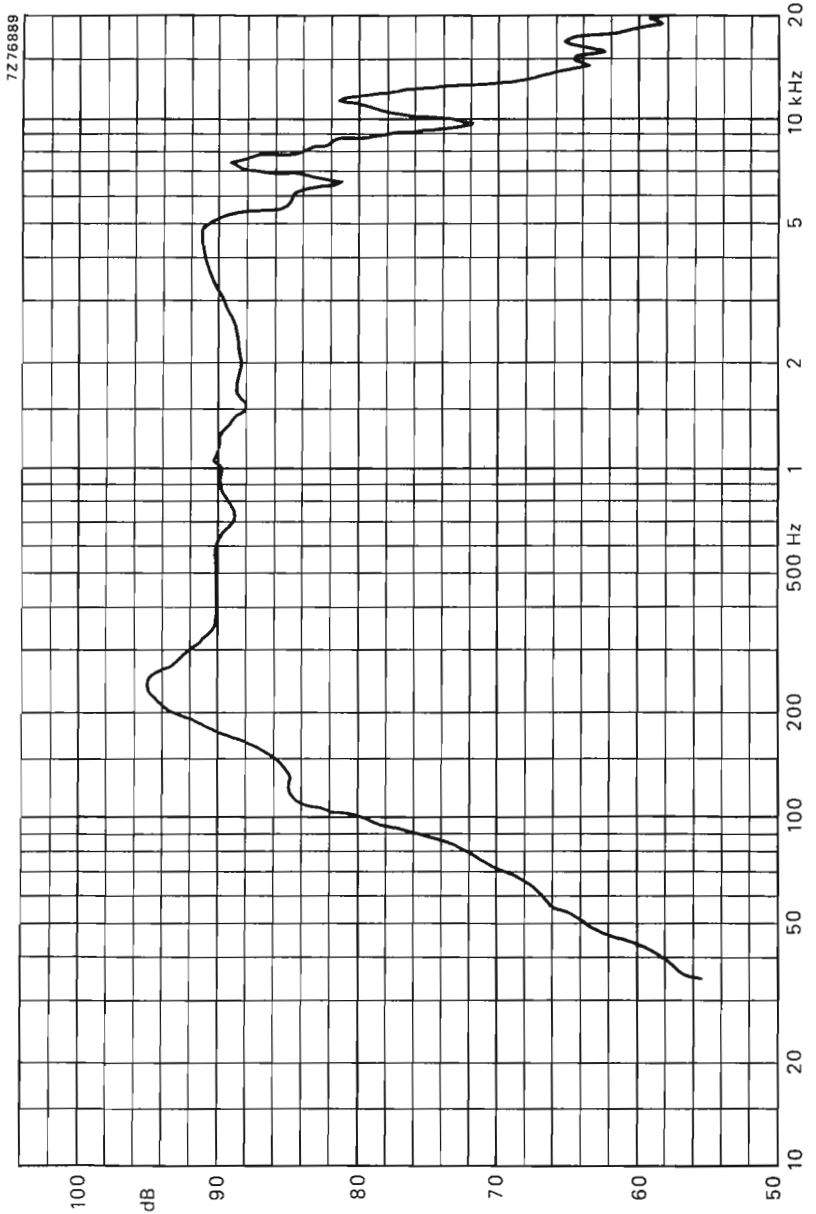


Fig. 2.

QUARTZ-CRYSTAL UNIT

Metal-plated AT-cut quartz plates for use as frequency standards in telephony systems.

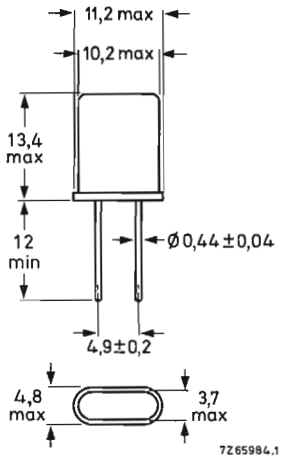
QUICK REFERENCE DATA

	144 04400	144 04290
Nominal frequency	3579,545 kHz	4782,143 kHz
Vibrational mode	fundamental	fundamental
Maximum adjustment tolerance	± 0,5%	± 0,5%
Maximum tolerance over temperature range −20 to + 70 °C (relative to frequency at 25 °C)	+ 0,01%	+ 0,005%
Appropriate mass	1 g	1 g

MECHANICAL DATA

Dimensions in mm

Outlines



16 DIGIT NUMERIC LIQUID-CRYSTAL-DISPLAY MODULE

The MB7020160 is a complete module including liquid-crystal display and two PCE 2111 drivers. Its serial data input is compatible with the I²C bus of the PCD 3340 (including software).

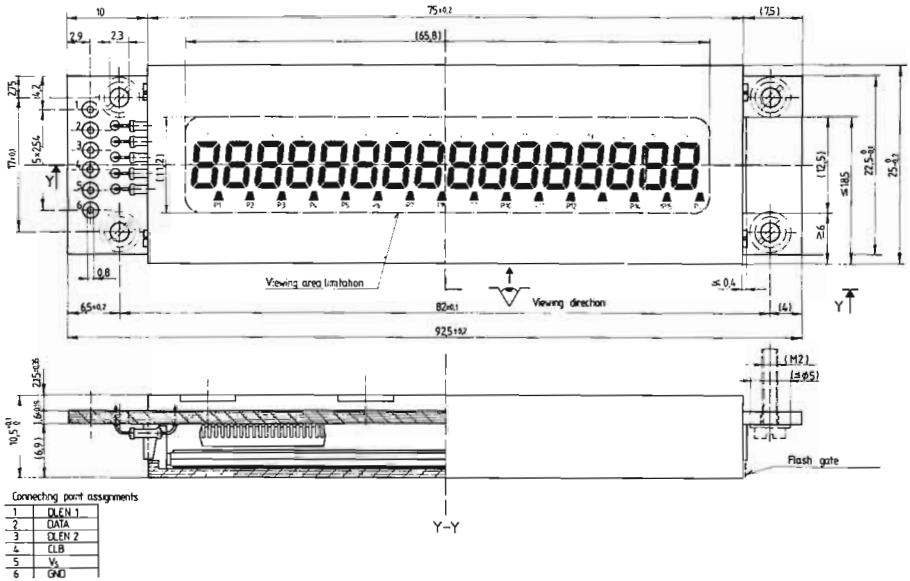
Features

- 16 seven-segment digits and decimal points
- good contrast over wide angular and temperature range
- automatic refresh of LCD
- low power consumption
- 6-wire connection to microcomputer (including supply)
- MUX 1 : 2, no temperature-compensation required
- LCDs protected by rugged transparent housing

QUICK REFERENCE DATA

Dimensions	92,5 x 25,0 x 10,5 mm³
Character height	6 mm
Operating voltage	typ. 3 V
Supply current	typ. 30 μA max. 100 μA

Product drawing



OTHER COMPONENTS FOR TELEPHONY

ISDN KIT

For the future Integrated-Services-Digital-Network (ISDN) an IC kit is in development. This will allow the formation of various digital telephone sets or terminals using a limited number of different components.

The terminal architecture is based on two internal buses: the I^2C bus for control and for packet-switched data, and the terminal highway for 64 kbit/s circuit-switched data (or digitized voice). These two buses interface with the subscriber line via a CCITT-compatible network termination. The same interface with the same flexibility can be used in the line card in the exchange.

Various function modules can be connected to the two buses, e.g. an audio module for the telephone function or a data module for a data terminal.

The terminal architecture is completed by the Integrated-Services-Terminal-bus interface circuit. The IST bus allows connection of an ISDN main terminal with up to 29 other terminals (including other main terminals).

Figure 1 shows how different types of terminal can be formed. Where no extension possibilities are required, the IST-bus interface circuit can be omitted (Fig. 1a). Fig. 1b shows how a main terminal with extension features can be formed, and Fig. 1c shows how to form an extension terminal without an interface to the subscriber line. As example, the first two can be telephone terminals and the third a data terminal.

Both internal and external traffic pass through the IST bus via the 8 x 64 kbit/s circuit-switched channels and the single 64 kbit/s signalling and packet-switched data channel. The IST-bus interface circuit together with the control unit (a standard microcomputer with peripherals like LCD and RAMs) acts as a distributed PABX.

One of the possible configurations is shown in Fig. 2 where the IST bus is used to create data islands as an extension of a digital PABX. Other possibilities are key-phone systems and Small Area Networks (SANs).

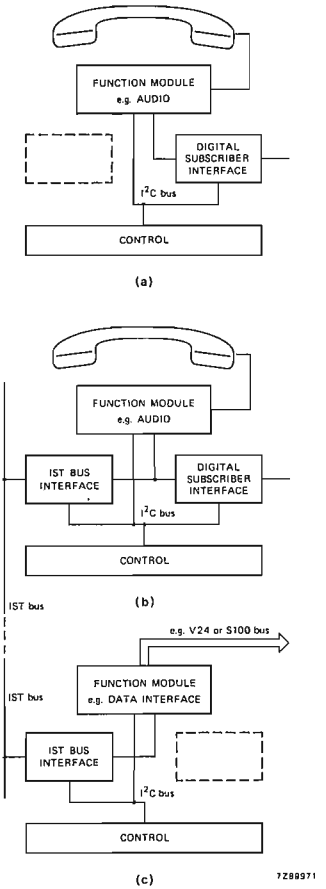


Fig. 1

a) main terminal without extension possibilities
b) main terminal
c) extension terminal via IST bus

OFFICE COMMUNICATION SYSTEM

(DATA-ISLAND: STAR/BUS COMBINATIONS)

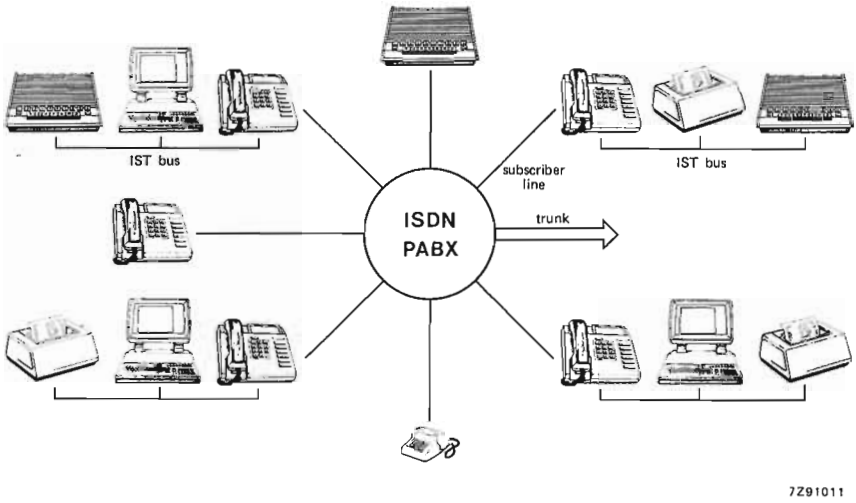


Fig. 2

IST-BUS INTERFACE CIRCUIT

The Integrated-Services-Terminal-bus interface circuit is a three-way interface function between the 1 Mbit/s IST bus, the 2 Mbit/s PCM terminal highway and the I²C-bus of the ISDN (up to 100 kbit/s). The 8 circuit-switched channels of the IST bus are interfaced with the terminal highway, and the packet-switched bd channel is interfaced with the I²C bus.

Features

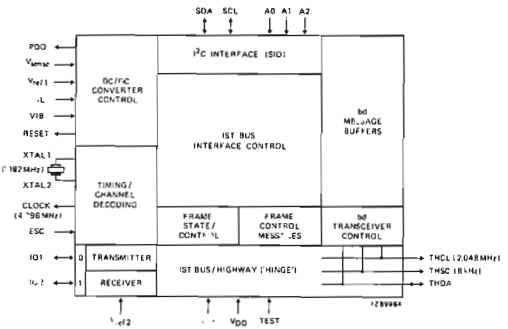
- single-chip interface with IST bus:
  - ⩽ 350 metre twisted pair
  - 8 x 64 kbit/s circuit-switched channels
  - 1 x 64 kbit/s packet-switched common signalling channel
- automatic frame word transmitter allocation
- CSMA/CD-ED bd-channel access protocol
- receiver input phase locked to IST-bus channels
- on-chip control circuit for a d.c./d.c. converter (terminal supply)
- power-on reset output

QUICK REFERENCE DATA

Supply voltage	typ. 5 V
Clock frequency	typ. 8,192 MHz
Clock output	typ. 4,096 MHz
Clock-rate on IST bus	typ. 1,024 MHz
Clock-rate on terminal highway	typ. 2,048 MHz
Frame synchronization frequency	typ. 8 kHz

Encapsulation: 24 pin DIL

BLOCK DIAGRAM



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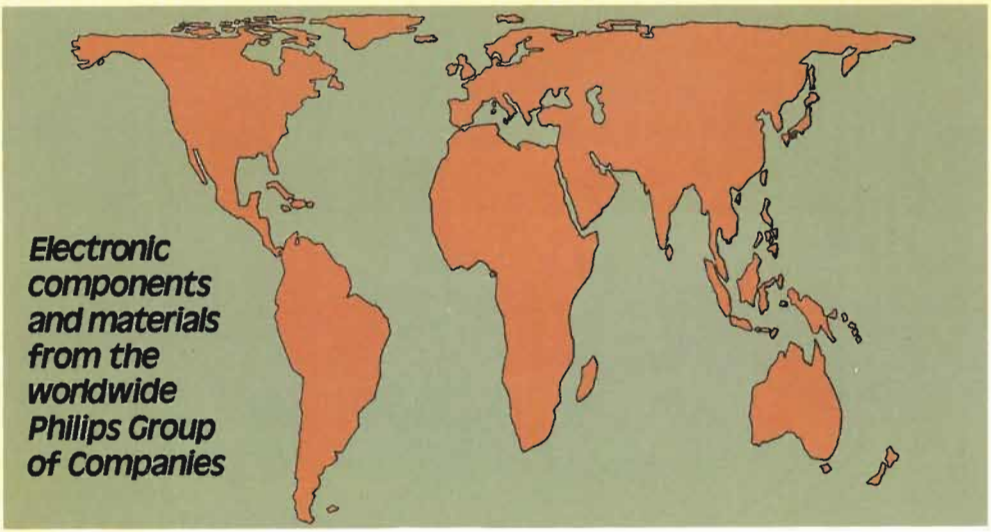

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